Extended Frequency Range (10 kHz to 300 kHz), Interleaving Continuous Conduction Mode PFC Controller

Check for Samples: UCC28070A

FEATURES

- **Interleaved Average Current-Mode PWM Control with Inherent Current Matching**
- **Advanced Current Synthesizer Current Sensing for Superior Efficiency**
- **Highly-Linear Multiplier Output with Internal Quantized Voltage Feed-Forward Correction for Near-Unity PF**
- **Extended Range Programmable Frequency (10 kHz to 300 kHz)**
- **Programmable Maximum Duty-Cycle Clamp**
- **Programmable Frequency Dithering Rate and Magnitude for Enhanced EMI Reduction**
  - **Magnitude: 3 kHz to 30 kHz**
  - **Rate: Up to 30 kHz**
- **External Clock Synchronization Capability**
- **Enhanced Load and Line Transient Response through Voltage Amplifier Output Slew-Rate Correction**
- **Programmable Peak Current Limiting**
- **Bias-Supply UVLO, Over-Voltage Protection, Open-Loop Detection, and PFC-Enable Monitoring**
- **External PFC-Disable Interface**
- **Open-Circuit Protection on VSENSE and VINAC pins**
- **Programmable Soft Start**
- **20-Lead TSSOP Package**

APPLICATIONS

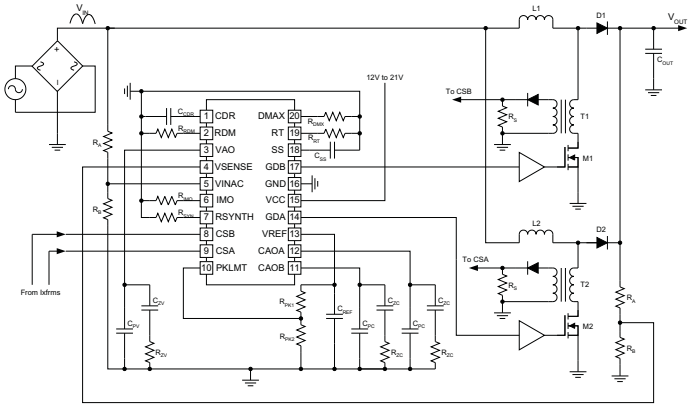
- **Air Conditioners and White Goods**
- **PFC Applications with IGBT Power Switches**
- **High-Efficiency Server and Desktop Power Supplies**
- **Telecom Rectifiers**
- **Industrial Equipment**

DESCRIPTION

The UCC28070A is an extended frequency range derivative of UCC28070, capable of operating at low switching frequencies desired for IGBT power switch based PFC converters in high power applications.

The UCC28070A is capable of operating in frequency range 10 kHz to 300 khz, thus extending the range of operation compared to UCC28070 whose minimum operating frequency was limited to 30 khz. All the other features and benefits of UCC28070 are also available in UCC28070A. The 180 degree out-of-phase interleaved operation generates substantial reduction in input and output ripple currents and conducted EMI filtering becomes easier and less expensive.

Simplified Application Diagram



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DESCRIPTION (CONT.)

Like UCC28070, UCC28070A also features multiple innovations including current synthesis and quantized voltage feed-forward to promote performance enhancements in PF, efficiency, THD, and transient response. Features including frequency dithering, clock synchronization, and slew rate enhancement further expand the potential performance enhancements. All protection features in UCC28070 such as output over-voltage detection, programmable peak-current limit, under-voltage lockout and open-loop protection are available in UCC28070A as well.

ORDERING INFORMATION

PART NUMBER	PACKAGE	PACKING
UCC28070APW	Plastic, 20-Pin TSSOP (PW)	70-Pc. Tube
UCC28070APWR	Plastic, 20-Pin TSSOP (PW)	2000-Pc. Tape and Reel

ABSOLUTE MAXIMUM RATINGS(1) (2) (3) (4)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	LIMIT	UNIT
Supply voltage: VCC	22	V
Supply current: I_{VCC}	20	mA
Voltage: GDA, GDB	−0.5 to VCC+0.3	V
Gate drive current – continuous: GDA, GDB	+/− 0.25	A
Gate drive current – pulsed: GDA, GDB	+/− 0.75	
Voltage: DMAX, RDM, RT, CDR, VINAC, VSENSE, SS, VAO, IMO, CSA, CSB, CAOA, CAOB, PKLMT, VREF	−0.5 to +7	V
Current: RT, DMAX, RDM, RSYNTH	−0.5	mA
Current: VREF, VAO, CAOA, CAOB, IMO	10	
Operating junction temperature, T_J	−40 to +125	°C
Storage temperature, T_{STG}	−65 to +150	
Lead temperature (10 seconds)	260	

(1) These are stress limits. Stress beyond these limits may cause permanent damage to the device. Functional operation of the device at these or any conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.
(2) All voltages are with respect to GND.
(3) All currents are positive into the terminal, negative out of the terminal.
(4) In normal use, terminals GDA and GDB are connected to an external gate driver and are internally limited in output current.

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ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	RATING	UNIT
Human Body Model (HBM)	2,000	V
Charged Device Model (CDM)	500	

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	MAX	UNIT
VCC Input Voltage (from a low-impedance source)	V_{UVLO} + 1 V	21	V
VREF Load Current		2	mA
VINAC Input Voltage Range	0	3	V
IMO Voltage Range	0	3.3	
PKLMT, CSA, & CSB Voltage Range	0	3.6	
RSYNTH Resistance (R_{SYN})	15	750	kΩ
RDM Resistance (R_{RDM})	30	330	

THERMAL INFORMATION

THERMAL METRIC(1)		PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)		°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)		
θ_{JB}	Junction-to-board thermal resistance(4)		
ψ_{JT}	Junction-to-top characterization parameter(5)		
ψ_{JB}	Junction-to-board characterization parameter(6)		
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)		

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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ELECTRICAL CHARACTERISTICS

over operating free-air temperature range −40°C < T_A < 125°C, T_J = T_A, VCC = 12 V, GND = 0 V, R_{RT} = 75 kΩ, R_{DMX} = 68.1 kΩ, R_{RDM} = R_{SYN} = 100 kΩ, C_{CDR} = 2.2 nF, C_{SS} = C_{VREF} = 0.1 µF, C_{VCC} = 1 µF, I_{VREF} = 0 mA (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Bias Supply						
VCC_{SHUNT}	VCC shunt voltage (1)	I_{VCC} = 10 mA	23	25	27	V
	VCC current, disabled	VSENSE = 0 V		7		mA
	VCC current, enabled	VSENSE = 3 V (switching)		9	12	
	VCC current, UVLO	VCC = 7 V			200	µA
		VCC = 9 V		4	6	mA
V_{UVLO}	UVLO turn-on threshold	Measured at VCC (rising)	9.8	10.2	10.6	V
	UVLO hysteresis	Measured at VCC (falling)		1		
	VREF enable threshold	Measured at VCC (rising)	7.5	8	8.5	
Linear Regulator						
	VREF voltage, no load	I_{VREF} = 0 mA	5.82	6	6.18	V
	VREF load rejection	Measured as the change in VREF, (I_{VREF} = 0 mA and −2 mA)	-12		12	mV
	VREF line rejection	Measured as the change in VREF, (VCC = 11V and 20 V, I_{VREF} = 0 µA)	-12		12	
PFC Enable						
V_{EN}	Enable threshold	Measured at VSENSE (rising)	0.65	0.75	0.85	V
	Enable hysteresis			0.15		
External PFC Disable						
	Disable threshold	Measured at SS (falling)	0.5	0.6		V
	Hysteresis	VSENSE > 0.85 V		0.15		
Oscillator						
	Output phase shift	Measured between GDA and GDB	179	180	181	Degree
V_{DMAX},V_{RT}, and V_{RDM}	Timing regulation voltages	Measured at DMAX, RT, & RDM	2.91	3	3.09	V
f_{PWM}	PWM switching frequency	R_{RT} = 750 kΩ, R_{DMX} = 681 kΩ, V_{RDM} = 0 V, V_{CDR} = 6 V	9.75	10.25	10.75	kHz
		R_{RT} = 75 kΩ, R_{DMX} = 68.1 kΩ, V_{RDM} = 0 V, V_{CDR} = 6 V	95	100	105	
		R_{RT} = 24.9 kΩ, R_{DMX} = 22.6 kΩ, V_{RDM} = 0 V, V_{CDR} = 6 V	270	290	330	
D_{MAX}	Duty-cycle clamp	R_{RT} = 75 kΩ, R_{DMX} = 68.1 kΩ, V_{RDM} = 0 V, V_{CDR} = 6 V	92%	95%	98%	
	Minimum programmable off-time	R_{RT} = 24.9 kΩ, R_{DMX} = 22.6 kΩ, V_{RDM} = 0 V, V_{CDR} = 6 V	50	150	250	ns
f_{DM}	Frequency dithering magnitude change in f_{PWM}	R_{RDM} = 316 kΩ, R_{RT} = 75 kΩ	2	3	4	kHz
		R_{RDM} = 31.6 kΩ, R_{RT} = 24.9 kΩ	24	30	36	
f_{DR}	Frequency dithering rate rate of change in f_{PWM}	C_{CDR} = 2.2 nF, R_{RDM} = 100 kΩ		3		
		C_{CDR} = 0.3 nF, R_{RDM} = 100 kΩ		20		
I_{CDR}	Dither rate current	Measure at CDR (sink and source)		±10		µA
	Dither disable threshold	Measured at C_{CDR} (rising)		5	5.25	V

(1) Excessive VCC input voltage and/or current damages the device. This clamp will not protect the device from an unregulated supply. If an unregulated supply is used, a series-connected fixed positive voltage regulator such as a UA78L15A is recommended. See the Absolute Maximum Ratings section for the limits on VCC voltage and current.

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ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range −40°C < T_A < 125°C, T_J = T_A, VCC = 12 V, GND = 0 V, R_{RT} = 75 kΩ, R_{DMX} = 68.1 kΩ, R_{RDM} = R_{SYN} = 100 kΩ, C_{CDR} = 2.2 nF, C_{SS} = C_{VREF} = 0.1 µF, C_{VCC} = 1 µF, I_{VREF} = 0 mA (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Clock Synchronization						
V_{CDR}	SYNC enable threshold	Measured at CDR (rising)		5	5.25	V
	SYNC propagation delay	V_{CDR} = 6 V, Measured from RDM (rising) to GDx (rising)		50	100	ns
	SYNC threshold (Rising)	V_{CDR} = 6 V, Measured at RDM		1.2	1.5	V
	SYNC threshold (Falling)	V_{CDR} = 6 V, Measured at RDM	0.4	0.7		
	SYNC pulses	Positive pulse width	0.2			µs
		Maximum duty cycle (2)		50		%
Voltage Amplifier						
	VSENSE voltage	In regulation, T_A = 25°C	2.97	3	3.03	V
	VSENSE voltage	In regulation	2.94	3	3.06	
	VSENSE input bias current	In regulation		250	500	nA
	VAO high voltage	VSENSE = 2.9 V	4.8	5	5.2	V
	VAO low voltage	VSENSE = 3.1 V		0.05	0.50	
g_{MV}	VAO transconductance	2.8 V < VSENSE < 3.2 V, VAO = 3 V		70		µS
	VAO sink current, overdriven limit	VSENSE = 3.5 V, VAO = 3 V		30		µA
	VAO source current, overdriven	VSENSE = 2.5 V, VAO = 3 V, SS = 3 V		−30		
	VAO source current, overdriven limit + I_{SRC}	VSENSE = 2.5 V, VAO = 3 V		−130		
	Slew-rate correction threshold	Measured as VSENSE (falling) / VSENSE (regulation)	92	93	95	%
	Slew-rate correction hysteresis	Measured at VSENSE (rising)		3	9	mV
I_{SRC}	Slew-rate correction current	Measured at VAO, in addition to VAO source current.		−100		µA
	Slew-rate correction enable threshold	Measured at SS (rising)		4		V
	VAO discharge current	VSENSE = 0.5 V, VAO = 1 V		10		µA
Soft Start						
I_{SS}	SS source current	VSENSE = 0.9 V, SS = 1 V		−10		µA
	Adaptive source current	VSENSE = 2.0 V, SS = 1 V		−1.5	-2.5	mA
	Adaptive SS disable	Measured as VSENSE – SS	-30	0	30	mV
	SS sink current	VSENSE = 0.5 V, SS = 0.2 V	0.5	0.9		mA

(2) Due to the influence of the synchronization pulse width on the programmability of the maximum PWM switching duty cycle (D_{MAX}) it is recommended to minimize the synchronization signal's duty cycle.

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ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range −40°C < T_A < 125°C, T_J = T_A, VCC = 12 V, GND = 0 V, R_{RT} = 75 kΩ, R_{DMX} = 68.1 kΩ, R_{RDM} = R_{SYN} = 100 kΩ, C_{CDR} = 2.2 nF, C_{SS} = C_{VREF} = 0.1 µF, C_{VCC} = 1 µF, I_{VREF} = 0 mA (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Over Voltage						
V_{OVP}	OVP threshold	Measured as VSENSE (rising) / VSENSE (regulation)	104	106	108	%
	OVP hysteresis	Measured at VSENSE (falling)		100		mV
	OVP propagation delay	Measured between VSENSE (rising) and GDx (falling)		0.2	0.3	µs
Zero-Power						
V_{ZPWR}	Zero-power detect threshold	Measured at VAO (falling)	0.65	0.75		V
	Zero-power hysteresis			0.15		
Multiplier						
k_{MULT}	Gain constant	VAO ≥ 1.5 V, T_A = 25°C	16	17	18	µA
		VAO = 1.2 V, T_A = 25°C	14.5	17.0	19.5	
		VAO ≥ 1.5 V	15	17	19	
		VAO = 1.2 V	13	17	21	
I_{IMO}	Output current: zero	VINAC = 0.9 V_{PK}, VAO = 0.8 V	-0.2	0	0.2	
		VINAC = 0 V, VAO = 5 V	-0.2	0	0.2	
Quantized Voltage Feed Forward						
V_{LVL1}	Level 1 threshold (3)	Measured at VINAC (rising)	0.6	0.7	0.8	V
V_{LVL2}	Level 2 threshold			1		
V_{LVL3}	Level 3 threshold			1.2		
V_{LVL4}	Level 4 threshold			1.4		
V_{LVL5}	Level 5 threshold			1.65		
V_{LVL6}	Level 6 threshold			1.95		
V_{LVL7}	Level 7 threshold			2.25		
V_{LVL8}	Level 8 threshold			2.6		
Current Amplifiers						
	CAOx high voltage		5.75	6		V
	CAOx low voltage				0.1	
g_{MC}	CAOx transconductance			100		µS
	CAOx sink current, overdriven			50		µA
	CAOx source current, overdriven			−50		
	Input common mode range		0		3.6	V
	Input offset Voltage	RSYNTH = 6 V, T_A = 25°C	-4	-8	-13	mV
		RSYNTH = 6 V	0	-8	-20	
	Input offset voltage		0	−8	−20	mV
	Phase mismatch	Measured as Phase A's input offset minus Phase B's input offset	-12	0	12	
	CAOx pull-down current	VSENSE = 0.5 V, CAOx = 0.2 V	0.5	0.9		mA

(3) The Level 1 threshold represents the "zero-crossing detection" threshold above which VINAC must rise to initiate a new input half-cycle, and below which VINAC must fall to terminate that half-cycle.

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ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range −40°C < T_A < 125°C, T_J = T_A, VCC = 12 V, GND = 0 V, R_{RT} = 75 kΩ, R_{DMX} = 68.1 kΩ, R_{RDM} = R_{SYN} = 100 kΩ, C_{CDR} = 2.2 nF, C_{SS} = C_{VREF} = 0.1 µF, C_{VCC} = 1 µF, I_{VREF} = 0 mA (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Synthesizer						
V_{RSYNTH}	Regulation voltage	VSENSE = 3 V, VINAC = 0 V	2.91	3	3.09	V
		VSENSE = 3 V, VINAC = 2.85 V	0.10	0.15	0.20	
	Synthesizer disable threshold	Measured at RSYNTH (rising)		5	5.25	
	VINAC input bias current			0.250	0.500	µA
Peak Current Limit						
	Peak current limit threshold	PKLMT = 3.30 V, measured at CSx (rising)	3.27	3.3	3.33	V
	Peak current limit propagation delay	Measured between CSx (rising) and GDx (falling) edges		60	100	ns
PWM Ramp						
V_{RMP}	PWM ramp amplitude		3.8	4.0	4.2	V
	PWM ramp offset voltage	T_A = 25°C, R_{RT} = 75 kΩ	0.65	0.7		
	PWM ramp offset temperature coefficient			−2		mV/ °C
Gate Drive						
	GDA, GDB output voltage, high, clamped	VCC = 20 V, C_{LOAD} = 1 nF	11.5	13	15	V
	GDA, GDB output voltage, High	C_{LOAD} = 1 nF	10	10.5		
	GDA, GDB output voltage, Low	C_{LOAD} = 1 nF		0.2	0.3	
	Rise time GDx	1 V to 9 V, C_{LOAD} = 1 nF		18	30	ns
	Fall time GDx	9 V to 1 V, C_{LOAD} = 1 nF		12	25	
	GDA, GDB output voltage, UVLO	VCC = 0 V, I_{GDA}, I_{GDB} = 2.5 mA		0.7	2	V
Thermal Shutdown						
	Thermal shutdown threshold			160		°C
	Thermal shutdown recovery			140		

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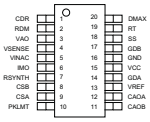
DEVICE INFORMATION

TSSOP-20 Top View, PW Package



TERMINAL FUNCTIONS

NAME	PIN #	I/O	DESCRIPTION
CDR	1	I	**Dither Rate Capacitor**. Frequency-dithering timing pin. An external capacitor to GND programs the rate of oscillator dither. Connect the CDR pin to the VREF pin to disable dithering.
RDM (SYNC)	2	I	**Dither Magnitude Resistor**. Frequency-dithering magnitude and external synchronization pin. An external resistor to GND programs the magnitude of oscillator frequency dither. When frequency dithering is disabled (CDR > 5 V), the internal master clock will synchronize to positive edges presented on the RDM pin. Connect RDM to GND when dithering is disabled and synchronization is not desired.
VAO	3	O	**Voltage Amplifier Output**. Output of transconductance voltage error amplifier. Internally connected to Multiplier input and Zero-Power comparator. Connect the voltage regulation loop compensation components between this pin and GND.
VSENSE	4	I	**Output Voltage Sense**. Internally connected to the inverting input of the transconductance voltage error amplifier in addition to the positive terminal of the Current Synthesis difference amplifier. Also connected to the OVP, PFC Enable, and slew-rate comparators. Connect to PFC output with a resistor-divider network.
VINAC	5	I	**Scaled AC Line Input Voltage**. Internally connected to the Multiplier and negative terminal of the Current Synthesis difference amplifier. Connect a resistor-divider network between V_{IN}, VINAC, and GND identical to the PFC output divider network connected at VSENSE.
IMO	6	O	**Multiplier Current Output**. Connect a resistor between this pin and GND to set the multiplier gain.
RSYNTH	7	I	**Current Synthesis Down-Slope Programming**. Connect a resistor between this pin and GND to set the magnitude of the current synthesizer down-slope. Connecting RSYNTH to VREF will disable current synthesis and connect CSA and CSB directly to their respective current amplifiers.
CSB	8	I	**Phase B Current Sense Input**. During the on-time of GDB, CSB is internally connected to the inverting input of Phase B's current amplifier through the current synthesis stage.
CSA	9	I	**Phase A Current Sense Input**. During the on-time of GDA, CSA is internally connected to the inverting input of Phase A's current amplifier through the current synthesis stage.
PKLMT	10	I	**Peak Current Limit Programming**. Connect a resistor-divider network between VREF and this pin to set the voltage threshold of the cycle-by-cycle peak current limiting comparators. Allows adjustment for desired ΔI_{LB}.

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TERMINAL FUNCTIONS (continued)

NAME	PIN #	I/O	DESCRIPTION
CAOB	11	O	**Phase B Current Amplifier Output**. Output of phase B's transconductance current amplifier. Internally connected to the inverting input of phase B's PWM comparator for trailing-edge modulation. Connect the current regulation loop compensation components between this pin and GND.
CAOA	12	O	**Phase A Current Amplifier Output**. Output of phase A's transconductance current amplifier. Internally connected to the inverting input of phase A's PWM comparator for trailing-edge modulation. Connect the current regulation loop compensation components between this pin and GND.
VREF	13	O	**6-V Reference Voltage and Internal Bias Voltage**. Connect a 0.1-µF ceramic bypass capacitor as close as possible to this pin and GND.
GDA	14	O	**Phase A's Gate Drive**. This limited-current output is intended to connect to a separate gate-drive device suitable for driving the Phase A switching component(s). The output voltage is typically clamped to 13.5 V.
VCC	15	I	**Bias Voltage Input**. Connect a 0.1-µF ceramic bypass capacitor as close as possible to this pin and GND.
GND	16	I/O	**Device Ground Reference**. Connect all compensation and programming resistor and capacitor networks to this pin. Connect this pin to the system through a separate trace for high-current noise isolation.
GDB	17	O	**Phase B's Gate Drive**. This limited-current output is intended to connect to a separate gate-drivedevice suitable for driving the Phase B switching component(s). The output voltage is typically clamped to 13.5 V.
SS	18	I	**Soft-Start and External Fault Interface**. Connect a capacitor to GND on this pin to set the soft-start slew rate based on an internally-fixed 10-µA current source. The regulation reference voltage for VSENSE is clamped to V_{SS} until V_{SS} exceeds 3 V. Upon recovery from certain fault conditions a 1-mA current source is present at the SS pin until the SS voltage equals the VSENSE voltage. Pulling the SS pin below 0.6 V immediately disables both GDA and GDB outputs.
RT	19	I	**Timing Resistor**. Oscillator frequency programming pin. A resistor to GND sets the running frequency of the internal oscillator.
DMAX	20	I	**Maximum Duty-Cycle Resistor**. Maximum PWM duty-cycle programming pin. A resistor to GND sets the PWM maximum duty-cycle based on the ratio of R_{DMX}/R_{RT}.

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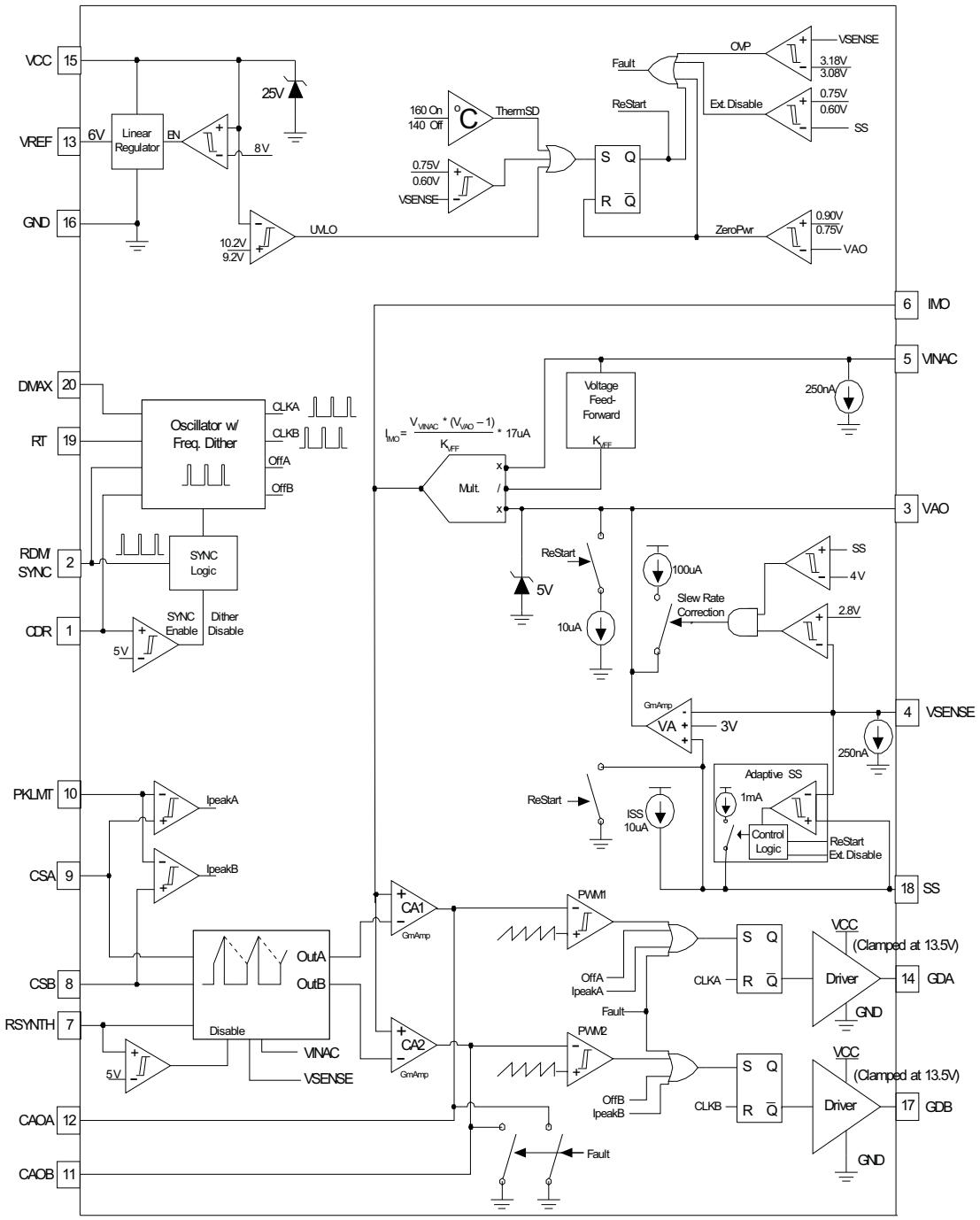
Functional Block Diagram



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TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs TEMPERATURE

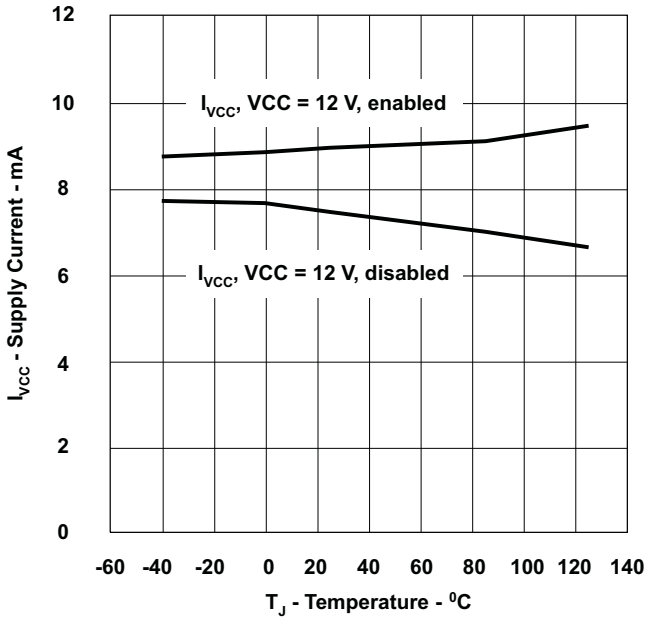

Figure 1.

REFERENCE VOLTAGE vs TEMPERATURE

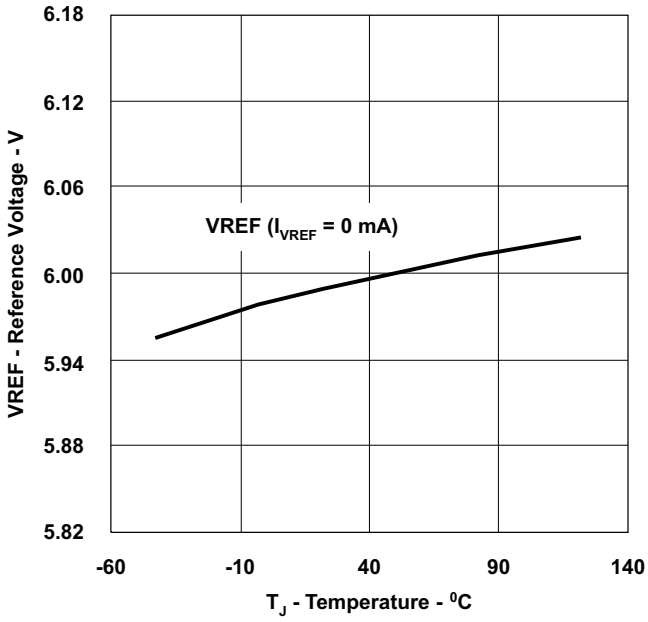

Figure 2.

VSENSE REGULATION vs TEMPERATURE

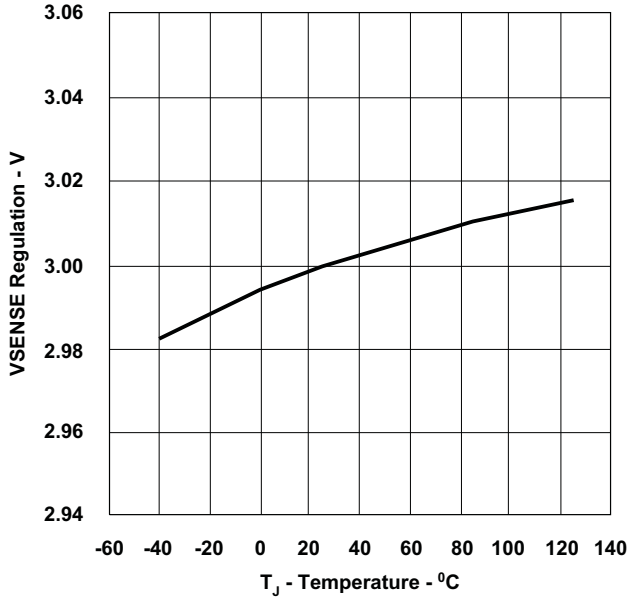

Figure 3.

I_{VSENSE} BIAS CURRENT vs TEMPERATURE

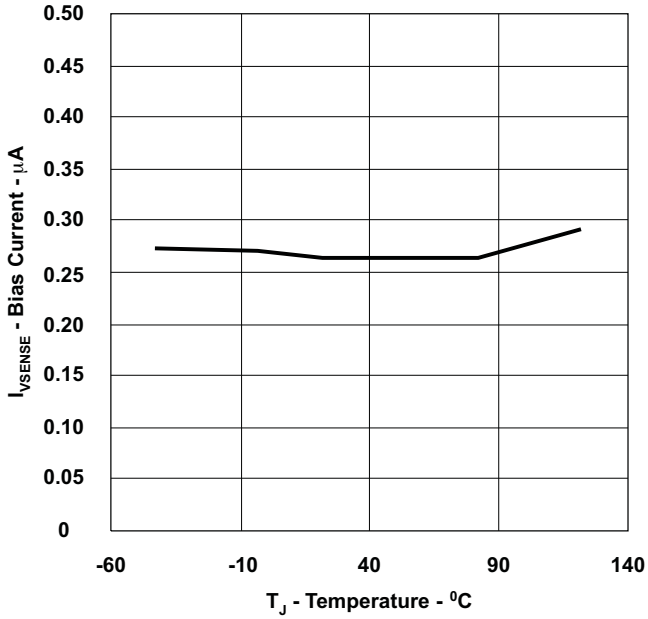

Figure 4.

TYPICAL CHARACTERISTICS (continued)

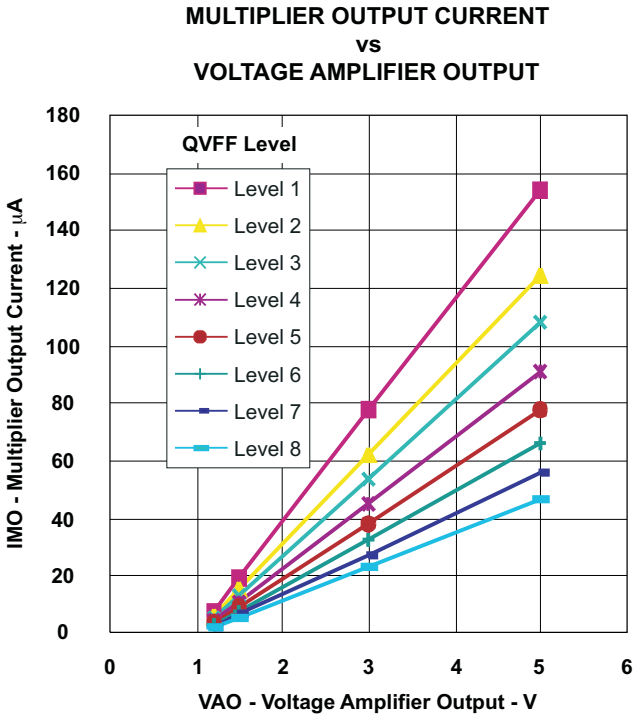

Figure 5.

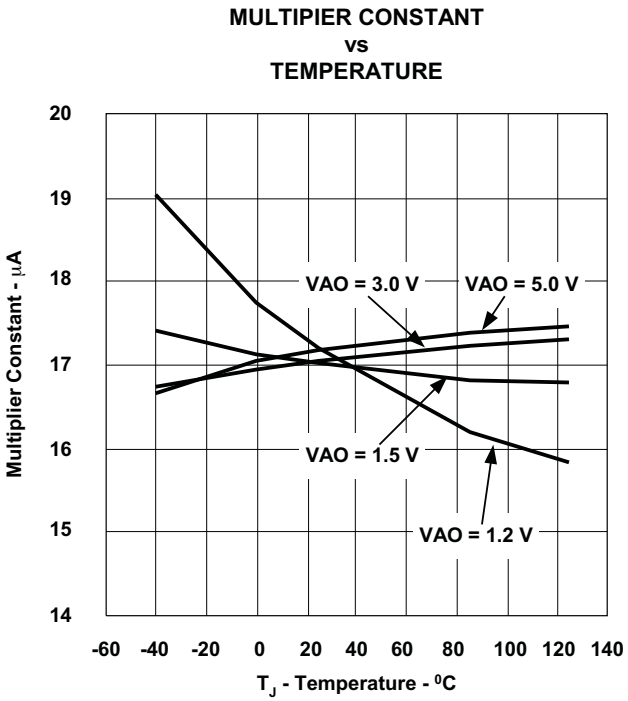

Figure 6.

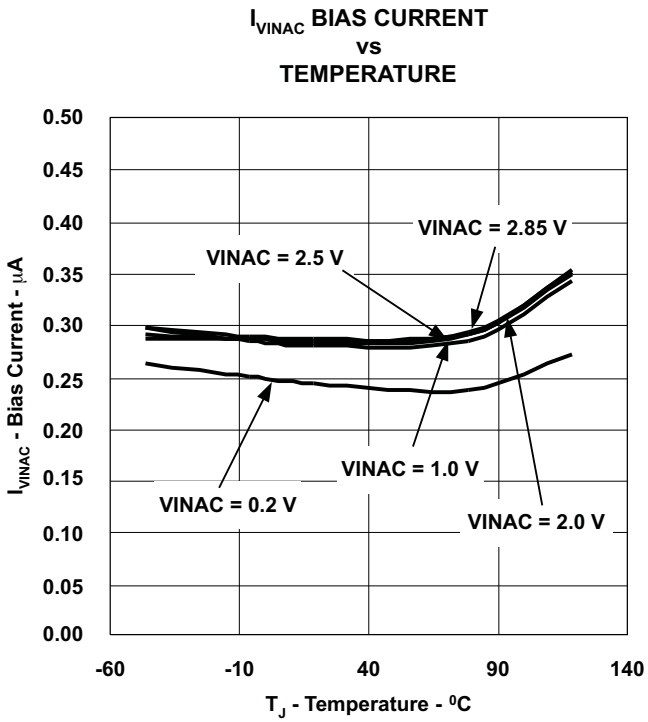

Figure 7.

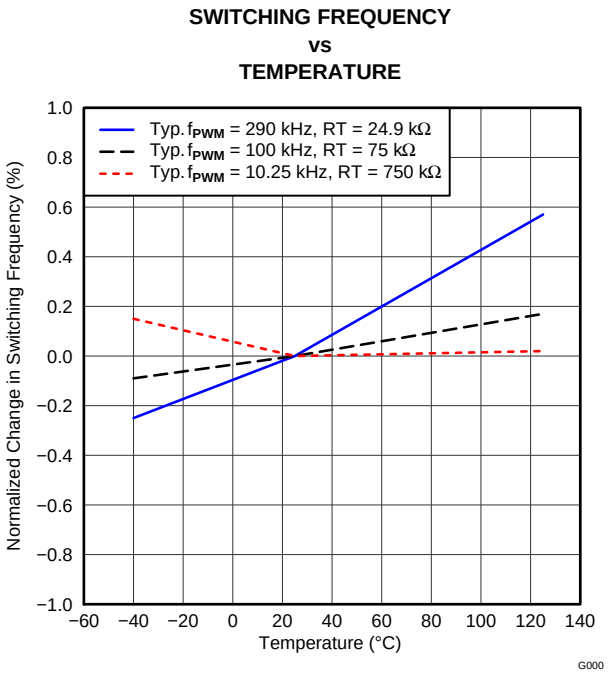

Figure 8.

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TYPICAL CHARACTERISTICS (continued)

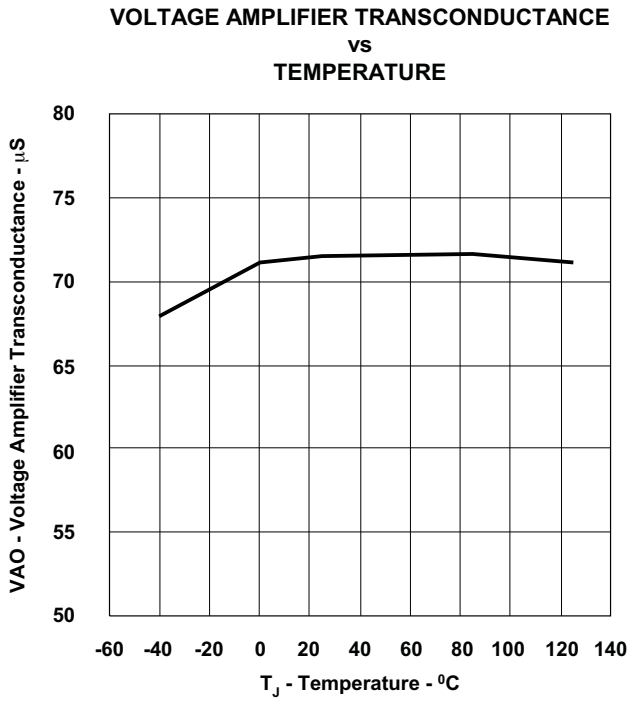

Figure 9.

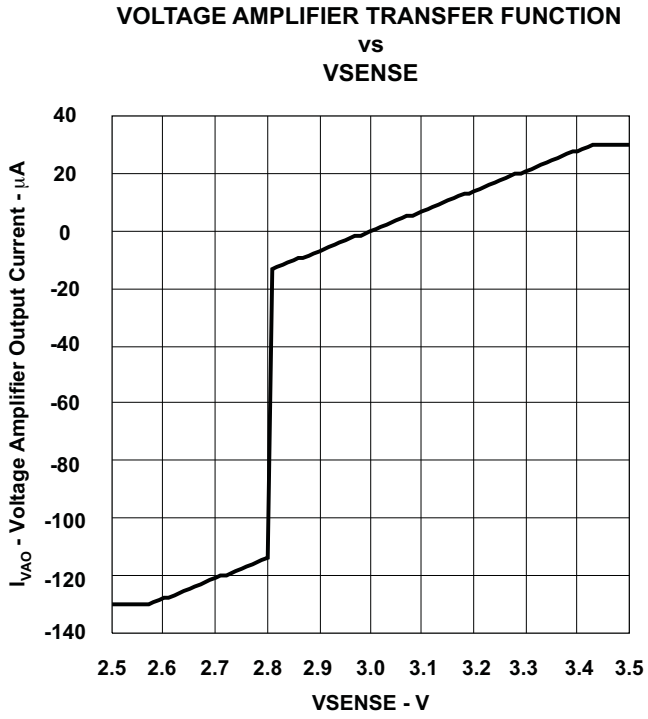

Figure 10.

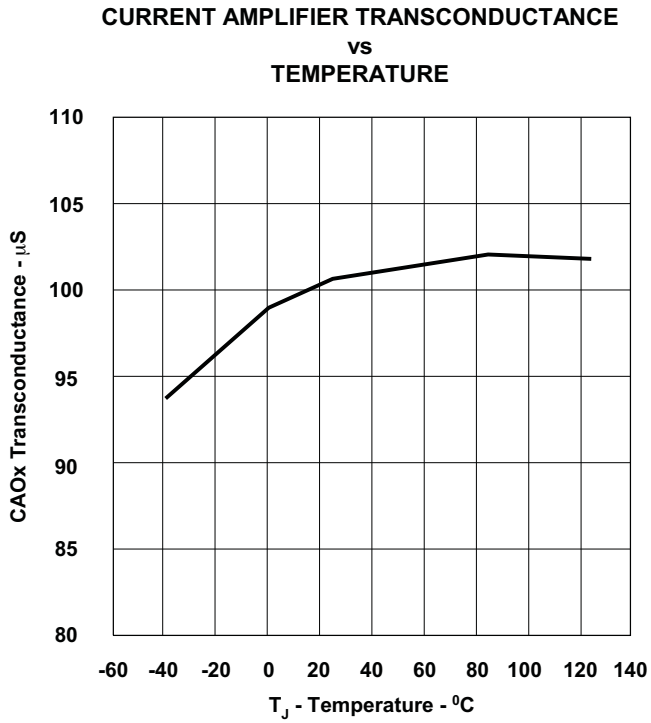

Figure 11.

TYPICAL CHARACTERISTICS (continued)

CAx INPUT OFFSET VOLTAGE vs TEMPERATURE (at 0.8 V common mode)

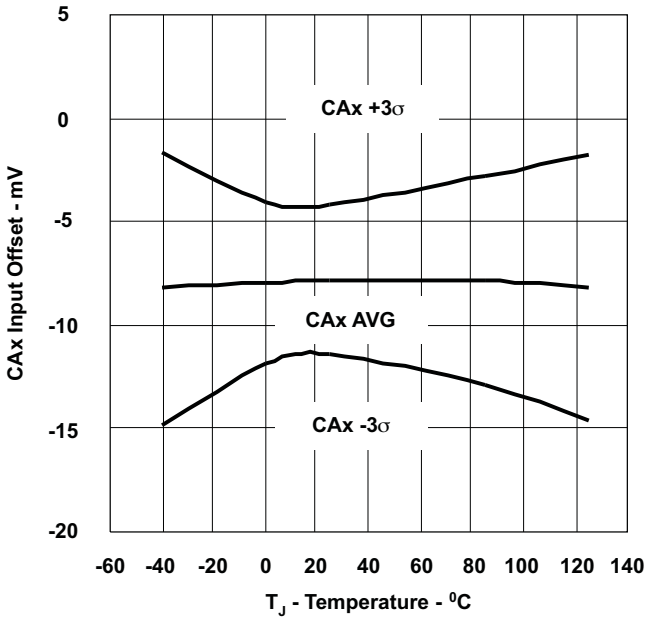

Figure 12.

CA1 TO CA2 RELATIVE OFFSET vs TEMPERATURE (at 0.8 V common mode)

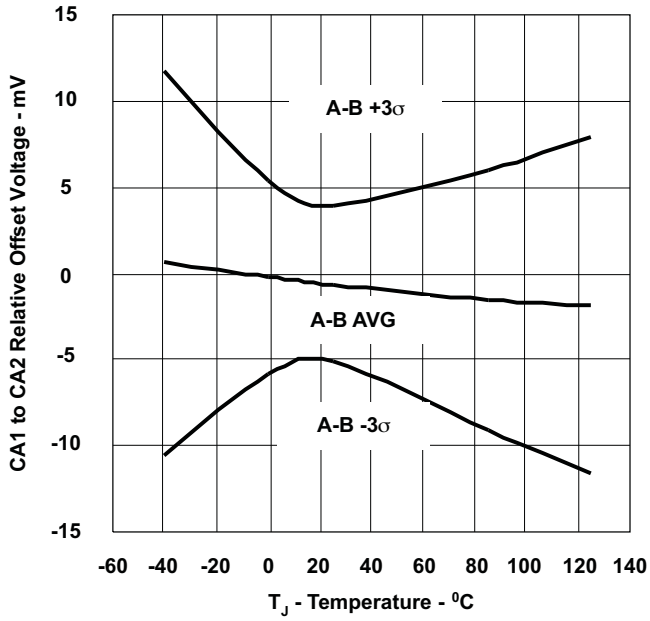

Figure 13.

CAx INPUT OFFSET VOLTAGE vs TEMPERATURE (at 2.0 V common mode)

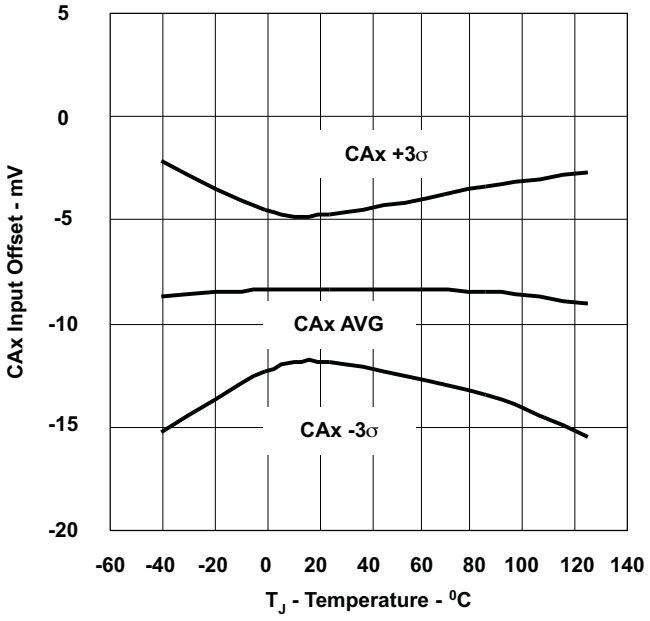

Figure 14.

CA1 TO CA2 RELATIVE OFFSET vs TEMPERATURE (at 2.0 V common mode)

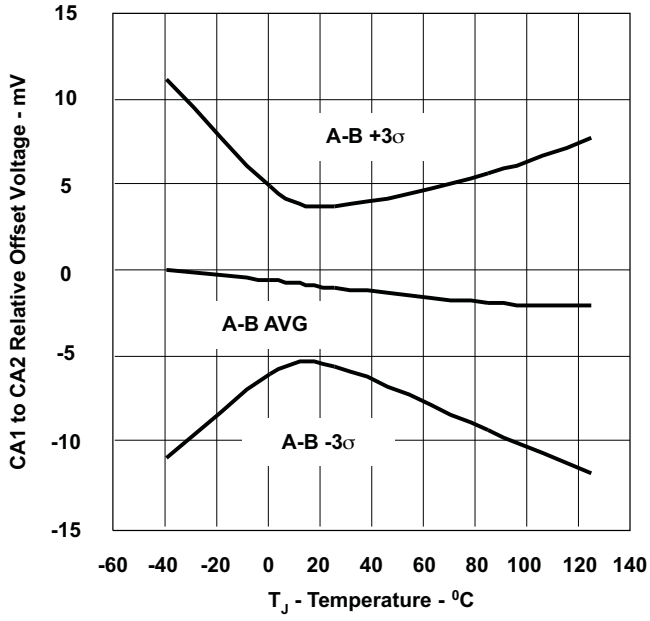

Figure 15.

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TYPICAL CHARACTERISTICS (continued)

CAx INPUT OFFSET VOLTAGE vs TEMPERATURE (at 3.6 V common mode)

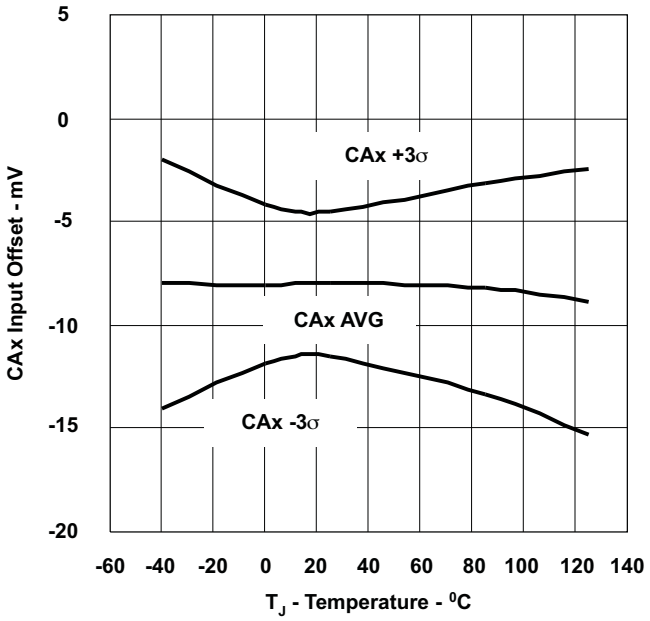

Figure 16.

CA1 TO CA2 RELATIVE OFFSET vs TEMPERATURE (at 3.6 V common mode)

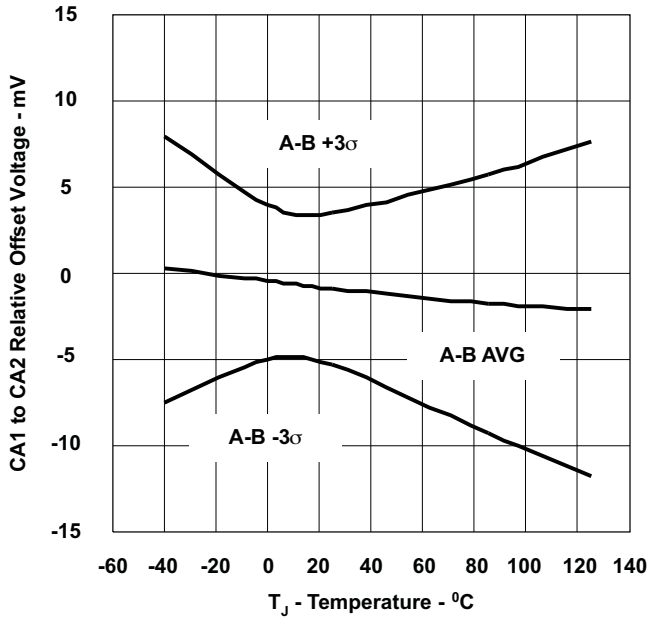

Figure 17.

APPLICATION INFORMATION

THEORY OF OPERATION

Interleaving

One of the main benefits from the 180° interleaving of phases is significant reductions in the high-frequency ripple components of both the input current and the current into the output capacitor of the PFC pre-regulator. Compared to that of a single-phase PFC stage of equal power, the reduced ripple on the input current eases the burden of filtering conducted-EMI noise and helps reduce the EMI filter and C_{IN} sizes. Additionally, reduced high-frequency ripple current into the PFC output capacitor, C_{OUT}, helps to reduce its size and cost. Furthermore, with reduced ripple and average current in each phase, the boost inductor size can be smaller than in a single-phase design [1].

Ripple current reduction due to interleaving is often referred to as “ripple cancellation”, but strictly speaking, the peak-to-peak ripple is completely cancelled only at 50% duty-cycle in a 2-phase system. At duty-cycles other than 50%, ripple reduction occurs in the form of partial cancellation due to the superposition of the individual phase currents. Nevertheless, compared to the ripple currents of an equivalent single-phase PFC pre-regulator, those of a 2-phase interleaved design are extraordinarily smaller [1]. Independent of ripple cancellation, the frequency of the interleaved ripple, at both the input and output, is 2 x f_{PWM}.

On the input, 180° interleaving reduces the peak-to-peak ripple amplitude to 1/2 or less of the ripple amplitude of the equivalent single-phase current.

On the output, 180° interleaving reduces the rms value of the PFC-generated ripple current in the output capacitor by a factor of slightly more than √2, for PWM duty-cycles > 50%.

This can be seen in the following derivations, adapting the method by Erickson [2].

In a single-phase PFC pre-regulator, the total rms capacitor current contributed by the PFC stage at all duty-cycles can be shown to be approximated by:

$$i_{CRMS1\varphi} = \left(\frac{I_O}{\eta}\right)\sqrt{\left(\left(\frac{16V_O}{3\pi V_M}\right) - \eta^2\right)} \quad (1)$$

In a dual-phase interleaved PFC pre-regulator, the total rms capacitor current contributed by the PFC stage for D > 50% can be shown to be approximated by:

$$i_{CRMS2\varphi} = \left(\frac{I_O}{\eta}\right)\sqrt{\left(\left(\frac{16V_O}{6\pi V_M}\right) - \eta^2\right)} \quad (2)$$

In these equations, I_O = average PFC output load current, V_O = average PFC output voltage, V_M = peak of the input ac-line voltage, and η = efficiency of the PFC stage at these conditions. It can be seen that the quantity under the radical for $i_{Crms2\varphi}$ is slightly smaller than 1/2 of that under the radical for $i_{Crms1\varphi}$. The rms currents shown contain both the low-frequency and the high-frequency components of the PFC output current. Interleaving reduces the high-frequency component, but not the low-frequency component.

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Programming the PWM Frequency and Maximum Duty-Cycle Clamp

The PWM frequency and maximum duty-cycle clamps for both GDx outputs of the UCC28070A are set through the selection of the resistors connected to the RT and DMAX pins, respectively. The selection of the RT resistor (R_{RT}) directly sets the PWM frequency (f_{PWM}).

$$R_{RT}\left(k\Omega\right)=\frac{7500}{f_{PWM}\left(kHz\right)} \tag{3}$$

Once R_{RT} has been determined, the D_{MAX} resistor (R_{DMX}) may be derived.

$$R_{DMX}=R_{RT}\times\left(2\times D_{MAX}-1\right) \tag{4}$$

where D_{MAX} is the desired maximum PWM duty-cycle.

Frequency Dithering (Magnitude and Rate)

Frequency dithering refers to modulating the switching frequency to achieve a reduction in conducted-EMI noise beyond the capability of the line filter alone. The UCC28070A implements a triangular modulation method which results in equal time spent at every point along the switching frequency range. This total range from minimum to maximum frequency is defined as the dither magnitude, and is centered around the nominal switching frequency f_{PWM} set with R_{RT}. For example, a dither magnitude of 20 kHz on a nominal f_{PWM} of 100 kHz results in a frequency range of 100 kHz ±10 kHz. Furthermore, the programmed duty-cycle clamp set by R_{DMX} remains constant at the programmed value across the entire range of the frequency dithering.

The rate at which f_{PWM} traverses from one extreme to the other and back again is defined as the dither rate. For example, a dither rate of 1 kHz would linearly modulate the nominal frequency from 110 kHz to 90 kHz to 110 kHz once every millisecond. A good initial design target for dither magnitude is ±10% of f_{PWM}. Most boost components can tolerate such a spread in f_{PWM}. The designer can then iterate around there to find the best compromise between EMI reduction, component tolerances, and loop stability.

The desired dither magnitude is set by a resistor from the RDM pin to GND, of value calculated by the following equation:

$$R_{RDM}\left(k\Omega\right)=\frac{937.5}{f_{DM}\left(kHz\right)} \tag{5}$$

Once the value of R_{RDM} is determined, the desired dither rate may be set by a capacitor from the CDR pin to GND, of value calculated by the following equation:

$$C_{CDR}\left(pF\right)=66.7\times\left(\frac{R_{RDM}\left(k\Omega\right)}{f_{DR}\left(kHz\right)}\right) \tag{6}$$

Frequency dithering may be fully disabled by forcing the CDR pin > 5 V or by connecting it to VREF (6 V) and connecting the RDM pin directly to GND. (If populated, the relatively high impedance of the RDM resistor may allow system switching noise to couple in and interfere with the controller timing functions if not bypassed with a low impedance path when dithering is disabled.)

If an external frequency source is used to synchronize f_{PWM} and frequency dithering is desired, the external frequency source must provide the dither magnitude and rate functions as the internal dither circuitry is disabled to prevent undesired performance during synchronization. (See following section for more details.)

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External Clock Synchronization

The UCC28070A has also been designed to be easily synchronized to almost any external frequency source. By disabling frequency dithering (pulling CDR > 5 V), the UCC28070A's SYNC circuitry is enabled permitting the internal oscillator to be synchronized with pulses presented on the RDM pin. In order to ensure a precise 180 degree phase shift is maintained between the GDA and GDB outputs, the frequency (f_{SYNC}) of the pulses presented at the RDM pin needs to be at twice the desired f_{PWM}. For example, if a 100-kHz switching frequency is desired, the f_{SYNC} should be 200 kHz.

$$f_{PWM} = \frac{f_{SYNC}}{2} \tag{7}$$

In order to ensure the internal oscillator does not interfere with the SYNC function, R_{RT} should be sized to set the internal oscillator frequency at least 10% below the f_{SYNC}.

$$R_{RT}\left(k\Omega\right) = \frac{15000}{f_{SYNC}\left(kHz\right)} \times 1.1 \tag{8}$$

It must be noted that the PWM modulator gain will be reduced by a factor equivalent to the scaled R_{RT} due to a direct correlation between the PWM ramp current and R_{RT}. Adjustments to the current loop gains should be made accordingly.

It must also be noted that the maximum duty cycle clamp programmability is affected during external synchronization. The internal timing circuitry responsible for setting the maximum duty cycle is initiated on the falling edge of the synchronization pulse. Therefore, the selection of R_{DMX} becomes dependent on the synchronization pulse width (t_{SYNC}).

$$D_{SYNC} = t_{SYNC} \times f_{SYNC}$$ For use in R_{DMX} equation immediately below. (9)

$$R_{DMX}\left(k\Omega\right) = \left(\frac{15000}{f_{SYNC}\left(kHz\right)}\right) \times \left(2 \times D_{MAX} - 1 - D_{SYNC}\right) \tag{10}$$

Consequently to minimize the impact of the t_{SYNC} it is clearly advantageous to utilize the smallest synchronization pulse width feasible.

NOTE

When external synchronization is used, a propagation delay of approximately 50 ns to 100 ns exists between internal timing circuits and the SYNC signal's falling edge, which may result in reduced off-time at the highest of switching frequencies. Therefore, R_{DMX} should be adjusted downward slightly by (T_{SYNC}-0.1 µs)/T_{SYNC} to compensate. At lower SYNC frequencies, this delay becomes an insignificant fraction of the PWM period, and can be neglected.

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Multi-phase Operation

External synchronization also facilitates using more than 2 phases for interleaving. Multiple UCC28070As can easily be paralleled to add an even number of additional phases for higher-power applications. With appropriate phase-shifting of the synchronization signals, even more input and output ripple current cancellation can be obtained. (An odd number of phases can be accommodated if desired, but the ripple cancellation would not be optimal.) For 4-, 6-, or any 2 x n-phases (where n = the number of UCC28070A controllers), each controller should receive a SYNC signal which is 360/n degrees out of phase with each other. For a 4-phase application interleaving with two controllers, SYNC1 should be 180° out of phase with SYNC2 for optimal ripple cancellation. Similarly for a 6-phase system, SYNC1, SYNC2, and SYNC3 should be 120° out of phase with each other for optimal ripple cancellation.

In a multi-phase interleaved system, each current loop is independent and treated separately, however there is only one common voltage loop. To maintain a single control loop, all VSENSE, VINAC, SS, IMO and VAO signals are paralleled, respectively between the n controllers. Where current-source outputs are combined (SS, IMO, VAO), the calculated load impedances must be adjusted by 1/n to maintain the same performance as with a single controller.

Figure 18 illustrates the paralleling of two controllers for a 4-phase 90°-interleaved PFC system.

VSENSE and VINAC Resistor Configuration

The primary purpose of the VSENSE input is to provide the voltage feedback from the output to the voltage control loop. Thus, a traditional resistor-divider network needs to be sized and connected between the output capacitor and the VSENSE pin to set the desired output voltage based on the 3-V regulation voltage on VSENSE.

A unique aspect of the UCC28070A is the need to place the same resistor-divider network on the V_{IN} side of the inductor to the VINAC pin. This provides the scaled input voltage monitoring needed for the linear multiplier and current synthesizer circuitry. It is not required that the actual resistance of the VINAC network be identical to the VSENSE network, but it is necessary that the attenuation (k_R) of the two divider networks be equivalent for proper PFC operation.

$$k_R = \frac{R_B}{\left(R_A + R_B\right)} \tag{11}$$

In noisy environments, it may be beneficial for small filter capacitors to be applied to the VSENSE and VINAC inputs to avoid the destabilizing effects of excessive noise on these inputs. If applied, the RC time-constant should not exceed 100µs on the VSENSE input to avoid significant delay in the output transient response. The RC time-constant should also not exceed 100 µs on the VINAC input to avoid degrading of the wave-shape zero-crossings. Usually, a time constant of $3/f_{PWM}$ is adequate to filter out typical noise on VSENSE and VINAC. Some design and test iteration may be required to find the optimal amount of filtering required in a particular application.

VSENSE and VINAC Open Circuit Protection

Both the VSENSE and VINAC pins have been designed with an internal 250-nA current sink to ensure that in the event of an open circuit at either pin, the voltage is not left undefined, and the UCC28070A remains in a “safe” operating mode.

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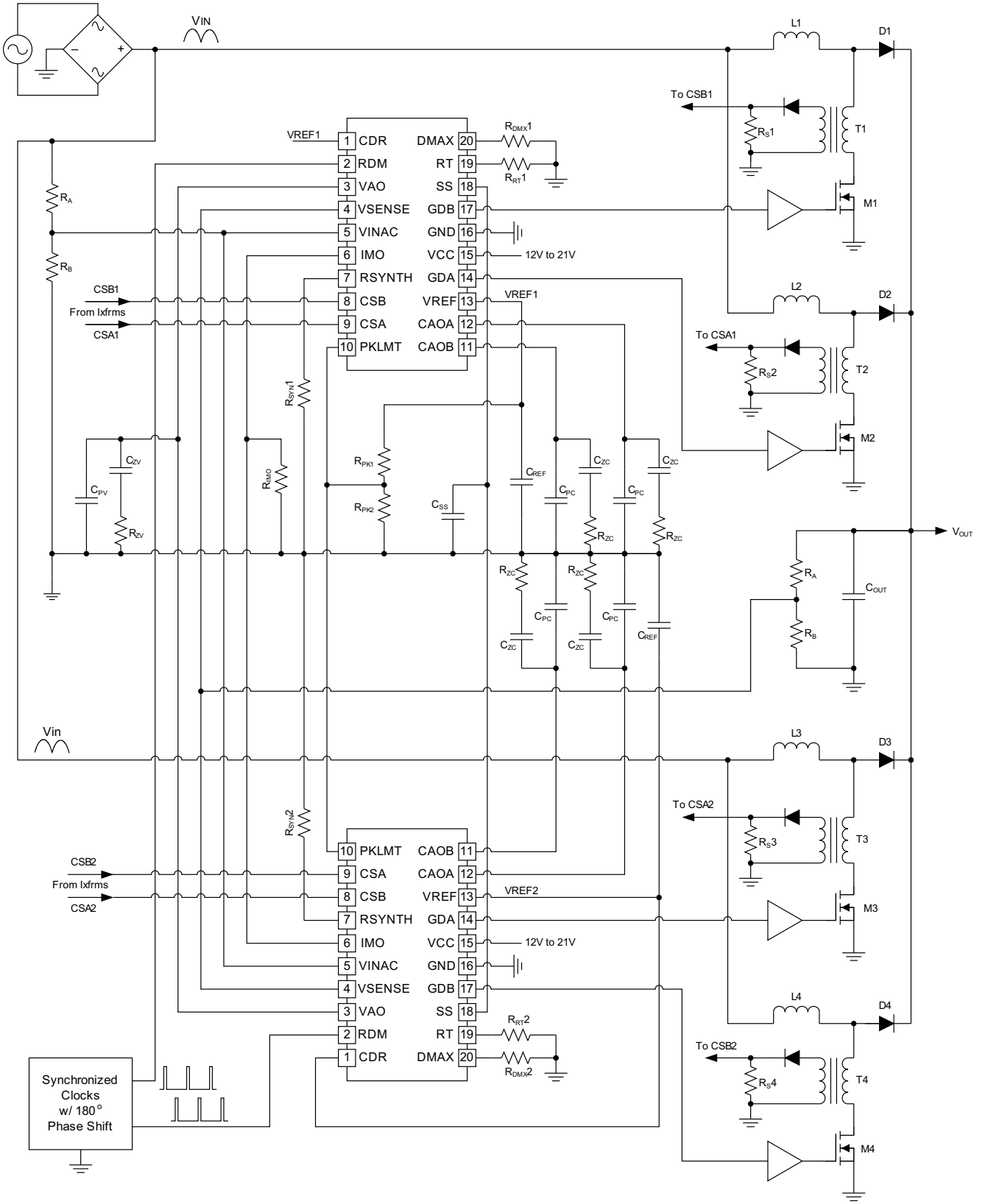

Figure 18. Simplified Four-Phase Application Diagram Using Two UCC28070A

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Current Synthesizer

One of the most prominent innovations in the UCC28070A design is the current synthesizer circuitry that synchronously monitors the instantaneous inductor current through a combination of on-time sampling and off-time down-slope emulation.

During the on-time of the GDA and GDB outputs, the inductor current is recorded at the CSA and CSB pins respectively via the current transformer network in each output phase. Meanwhile, the continuous monitoring of the input and output voltage via the VINAC and VSENSE pins permits the UCC28070A to internally recreate the inductor current's down-slope during each output's respective off-time. Through the selection of the RSYNTH resistor (R_{SYN}), based on the equation below, the internal response may be adjusted to accommodate the wide range of inductances expected across the wide array of applications.

During inrush surge events at power-up and ac drop-out recovery, VSENSE < VINAC, so the synthesized down slope becomes zero. In this case, the synthesized inductor current will remain above the IMO reference and the current loop drives the duty cycle to zero. This avoids excessive stress on the MOSFETS during the surge event. Once VINAC falls below VSENSE the duty cycle increases until steady-state operation resumes.

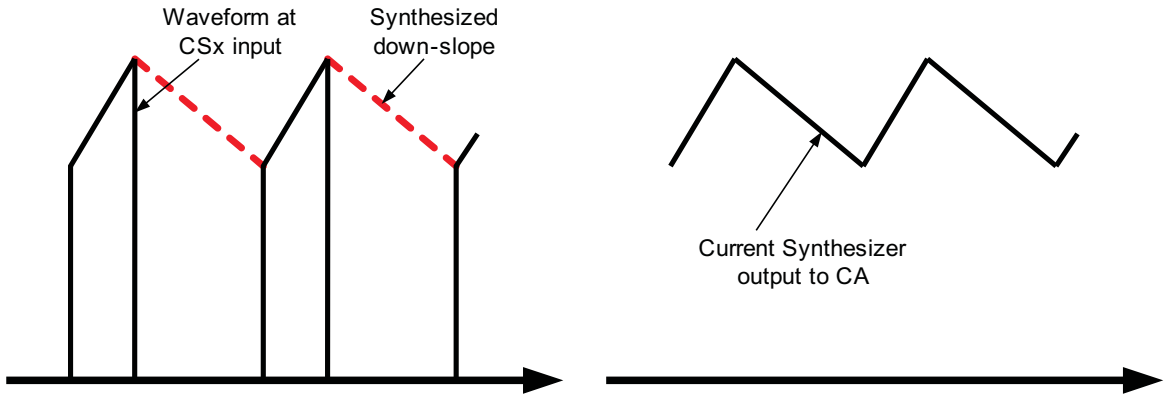

Figure 19. Inductor Current's Down Slope

$$R_{SYN}\left(k\Omega\right)=\frac{\left(10\times N_{CT}\times L_B\left(\mu H\right)\times k_R\right)}{R_S\left(\Omega\right)} \tag{12}$$

Variables

- L_B = Nominal Zero-Bias Boost Inductance (µH),
- R_S = Sense Resistor (Ω),
- N_{CT} = Current-sense Transformer turns ratio,
- $k_R = R_B/(R_A+R_B)$ = the resistor-divider attenuation at the VSENSE and VINAC pins.

Programmable Peak Current Limit

The UCC28070A has been designed with a programmable cycle-by-cycle peak current limit dedicated to disabling either GDA or GDB output whenever the corresponding current-sense input (CSA or CSB respectively) rises above the voltage established on the PKLMT pin. Once an output has been disabled via the detection of peak current limit, the output remains disabled until the next clock cycle initiates a new PWM period. The programming range of the PKLMT voltage extends to upwards of 4 V to permit the full utilization of the 3-V average current sense signal range, however it should be noted that the linearity of the current amplifiers begin to compress above 3.6 V.

A resistor-divider network from VREF to GND can easily program the peak current limit voltage on PKLMT, provided the total current out of VREF is less than 2 mA to avoid drooping of the 6-V VREF voltage. A load of less than 0.5 mA is suggested, but if the resistance on PKLMT is very high, a small filter capacitor on PKLMT is recommended to avoid operational problems in high-noise environments.

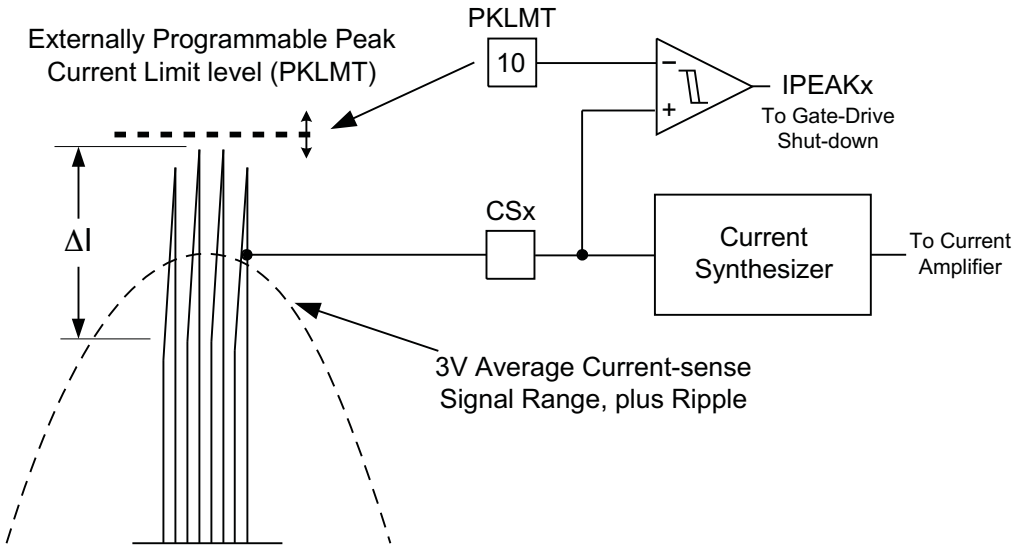

Figure 20. Externally Programmable Peak Current Limit

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Linear Multiplier

The multiplier of the UCC28070A generates a reference current which represents the desired wave shape and proportional amplitude of the ac input current. This current is converted to a reference voltage signal by the R_{IMO} resistor, which is scaled in value to match the voltage of the current-sense signals. The instantaneous multiplier current is dependent upon the rectified, scaled input voltage V_{VINAC} and the voltage-error amplifier output V_{VAO}. The V_{VINAC} signal conveys three pieces of information to the multiplier:

1. The overall wave-shape of the input voltage (typically sinusoidal),
2. The instantaneous input voltage magnitude at any point in the line cycle,
3. The rms level of the input voltage.

The V_{VAO} signal represents the total output power of the PFC pre-regulator.

A major innovation in the UCC28070A multiplier architecture is the internal quantized V_{RMS} feed-forward (Q_{VFF}) circuitry, which eliminates the requirement for external filtering of the VINAC signal and the subsequent slow response to transient line variations. A unique circuit algorithm detects the transition of the peak of V_{VINAC} through seven thresholds and generates an equivalent VFF level centered within the eight Q_{VFF} ranges. The boundaries of the ranges expand with increasing V_{IN} to maintain an approximately equal-percentage delta between levels. These eight Q_{VFF} levels are spaced to accommodate the full “universal” line range of 85 V-265 V_{RMS}.

A great benefit of the Q_{VFF} architecture is that the fixed k_{VFF} factors eliminate any contribution to distortion of the multiplier output, unlike an externally-filtered VINAC signal which unavoidably contains 2nd-harmonic distortion components. Furthermore, the Q_{VFF} algorithm allows for rapid response to both increasing and decreasing changes in input rms voltage so that disturbances transmitted to the PFC output are minimized. 5% hysteresis in the level thresholds help avoid “chattering” between Q_{VFF} levels for V_{VINAC} voltage peaks near a particular threshold or containing mild ringing or distortion. The Q_{VFF} architecture requires that the input voltage be largely sinusoidal, and relies on detecting zero-crossings to adjust Q_{VFF} downward on decreasing input voltage. Zero-crossings are defined as V_{VINAC} falling below 0.7 V for at least 50 µs typically.

Table 1 reflects the relationship between the various VINAC peak voltages and the corresponding k_{VFF} terms for the multiplier equation.

Table 1. VINAC Peak Voltages

LEVEL	V_{VINAC} PEAK VOLTAGE	k_{VFF} (V^2)	V_{IN} PEAK VOLTAGE (1)
8	2.60 V ≤ $V_{VINAC(pk)}$	3.857	> 345 V
7	2.25 V ≤ $V_{VINAC(pk)}$ < 2.60 V	2.922	300 V to 345 V
6	1.95 V ≤ $V_{VINAC(pk)}$ < 2.25 V	2.199	260 V to 300 V
5	1.65 V ≤ $V_{VINAC(pk)}$ < 1.95 V	1.604	220 V to 260 V
4	1.40 V ≤ $V_{VINAC(pk)}$ < 1.65 V	1.156	187 V to 220 V
3	1.20 V ≤ $V_{VINAC(pk)}$ < 1.40 V	0.839	160 V to 187 V
2	1.00 V ≤ $V_{VINAC(pk)}$ < 1.20 V	0.600	133 V to 160 V
1	$V_{VINAC(pk)}$ ≤ 1.00 V	0.398	< 133 V

(1) The V_{IN} peak voltage boundary values listed above are calculated based on a 400-V PFC output voltage and the use of a matched resistor-divider network (k_R = 3 V/400 V = 0.0075) on VINAC and VSENSE (as required for current synthesis). When V_{OUT} is designed to be higher or lower than 400 V, k_R = 3 V/V_{OUT}, and the V_{IN} peak voltage boundary values for each Q_{VFF} level adjust to $V_{VINAC(pk)}/k_R$.

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The multiplier output current I_{IMO} for any line and load condition can thus be determined by the equation

$$I_{IMO} = \frac{17\mu A \times (V_{VINAC}) \times (V_{VAO} - 1)}{k_{VFF}} \quad (13)$$

Because the k_{VFF} value represents the scaled V_{RMS}^2 at the center of a level, V_{VAO} will adjust slightly upwards or downwards when $VINAC_{pk}$ is either lower or higher than the center of the Q_{VFF} voltage range to compensate for the difference. This is automatically accomplished by the voltage loop control when V_{IN} varies, both within a level and after a transition between levels.

The output of the voltage-error amplifier VAO is clamped at 5.0 V, which represents the maximum PFC output power. This value is used to calculate the maximum reference current at the IMO pin, and sets a limit for the maximum input power allowed (and, as a consequence, limits maximum output power).

Unlike a continuous V_{FF} situation, where maximum input power is a fixed power at any V_{RMS} input, the discrete Q_{VFF} levels permit a variation in maximum input power within limited boundaries as the input V_{RMS} varies within each level.

The lowest maximum power limit occurs at the VINAC voltage of 0.76 V, while the highest maximum power limit occurs at the increasing threshold from level-1 to level-2. This pattern repeats at every level transition threshold, keeping in mind that decreasing thresholds are 95% of the increasing threshold values. Below VINAC = 0.76 V, P_{IN} is always less than $P_{IN(max)}$, falling linearly to zero with decreasing input voltage.

For example, to design for the lowest maximum power allowable, determine the maximum steady-state (average) output power required of the PFC pre-regulator and add some additional percentage to account for line drop-out recovery power (to recharge C_{OUT} while full load power is drawn) such as 10% or 20% of $P_{OUT(max)}$. Then apply the expected efficiency factor to find the lowest maximum input power allowable:

$$P_{IN(max)} = \frac{1.10 \times P_{OUT(max)}}{\eta} \quad (14)$$

At the $P_{IN(max)}$ design threshold, V_{VINAC} = 0.76 V, hence Q_{VFF} = 0.398 and input V_{AC} = 73 V_{RMS} (accounting for 2-V bridge-rectifier drop) for a nominal 400-V output system.

$$\text{Thus } I_{IN(rms)} = \frac{P_{IN(max)}}{73V_{RMS}}, \text{ and } I_{IN(pk)} = 1.414 \times I_{IN(rms)} \quad (15)$$

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This $I_{IN(pk)}$ value represents the combined average current through the boost inductors at the peak of the line voltage. Each inductor current is detected and scaled by a current-sense transformer (CT). Assuming equal currents through each interleaved phase, the signal voltage at each current sense input pin (CSA and CSB) is developed across a sense resistor selected to generate ~3 V based on (1/2) x $I_{IN(pk)}$ x R_S/N_{CT}, where R_S is the current sense resistor and N_{CT} is the CT turns-ratio.

I_{IMO} is then calculated at that same lowest maximum-power point, as

$$I_{IMO(max)} = 17\mu A \times \frac{(0.76V)(5V - 1V)}{0.398} = 130\mu A \tag{16}$$

R_{IMO} is selected such that:

$$R_{IMO} \times I_{IMO(max)} = \left(\frac{1}{2}\right) \times I_{IN(pk)} \times \frac{R_S}{N_{CT}} \tag{17}$$

Therefore:

$$R_{IMO} = \frac{\left(\left(\frac{1}{2}\right) \times I_{IN(pk)} \times R_S\right)}{\left(N_{CT} \times I_{IMO(max)}\right)} \tag{18}$$

At the increasing side of the level-1 to level-2 threshold, it should be noted that the IMO current would allow higher input currents at low-line:

$$I_{IMO(L1-L2)} = 17\mu A \times \frac{(1.0V)(5V - 1V)}{0.398} = 171\mu A \tag{19}$$

However, this current may easily be limited by the programmable peak current limiting (PKLMT) feature of the UCC28070A if required by the power stage design.

The same procedure can be used to find the lowest and highest input power limits at each of the Q_{VFF} level transition thresholds. At higher line voltages, where the average current with inductor ripple is traditionally below the PKLMT threshold, the full variation of maximum input power will be seen, but the input currents will inherently be below the maximum acceptable current levels of the power stage.

The performance of the multiplier in the UCC28070A has been significantly enhanced when compared to previous generation PFC controllers, with high linearity and accuracy over most of the input ranges. The accuracy is at its worst as V_{VAO} approaches 1 V because the error of the (V_{VAO}-1) subtraction increases and begins to distort the IMO reference current to a greater degree.

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Enhanced Transient Response (VA Slew-Rate Correction)

Due to the low voltage loop bandwidth required to maintain proper PFC and ignore the slight 120-Hz ripple on the output, the response of ordinary controllers to input voltage and load transients will also be slow. However, the Q_{VFF} function effectively handles the line transient response with the exception of any minor adjustments needed within a Q_{VFF} level. Load transients on the other hand can only be handled by the voltage loop, therefore, the UCC28070A has been designed to improve its transient response by pulling up on the output of the voltage amplifier (VAO) with an additional 100 µA of current in the event the VSENSE voltage drops below 93% of regulation (2.79 V). During a soft-start cycle, when VSENSE is ramping up from the 0.75-V PFC Enable threshold, the 100-µA correction current source is disabled to ensure the gradual and controlled ramping of output voltage and current during a soft start.

Voltage Biasing (VCC and VREF)

The UCC28070A operates within a VCC bias supply range of 10 V to 21 V. An Under-Voltage Lock-Out (UVLO) threshold prevents the PFC from activating until VCC > 10.2 V, and 1 V of hysteresis assures reliable start-up from a possibly low-compliance bias source. An internal 25-V zener-like clamp on VCC is intended only to protect the device from brief energy-limited surges from the bias supply, and should NOT be used as a regulator with a current-limited source.

At minimum, a 0.1-µF ceramic bypass capacitor must be applied from VCC to GND close to the device pins to provide local filtering of the bias supply. Larger values may be required depending on I_{CC} peak current magnitudes and durations to minimize ripple voltage on VCC.

In order to provide a smooth transition out of UVLO and to make the 6-V voltage reference available as early as possible, the VREF output is enabled when VCC exceeds 8 V typically.

The VREF circuitry is designed to provide the biasing of all internal control circuits and for limited use externally. At minimum, a 22-nF ceramic bypass capacitor must be applied from VREF to GND close to the device pins to ensure stability of the circuit. External load current on VREF should be limited to less than 2 mA, or degraded regulation may result.

PFC Enable and Disable

The UCC28070A contains two independent circuits dedicated to disabling the GDx outputs based on the biasing conditions of the VSENSE or SS pins. The first circuit which monitors the V_{VSENSE}, is the traditional PFC Enable that holds off soft-start and the overall PFC function until the output has pre-charged to ~25%. Prior to V_{VSENSE} reaching 0.75 V, almost all of the internal circuitry is disabled. Once V_{VSENSE} reaches 0.75 V and VAO < 0.75 V, the oscillator, multiplier, and current synthesizer are enabled and the SS circuitry begins to ramp up the voltage on the SS pin. The second circuit provides an external interface to emulate an internal fault condition to disable the GDx output without fully disabling the voltage loop and multiplier. By externally pulling the SS pin below 0.6 V, the GDx outputs are immediately disabled and held low. Assuming no other fault conditions are present, normal PWM operation resumes when the external SS pull-down is released. It must be noted that the external pull-down needs to be sized large enough to override the internal 1.5-mA adaptive SS pull-up once the SS voltage falls below the disable threshold. It is recommended that a MOSFET with less than 100-Ω $R_{DS(on)}$ resistance be used to ensure the SS pin is held adequately below the disable threshold.

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Adaptive Soft Start

In order to maintain a controlled power up, the UCC28070A has been designed with an adaptive soft-start function that overrides the internal reference voltage with a controlled voltage ramp during power up. On initial power up, once V_{VSENSE} exceeds the 0.75-V enable threshold (V_{EN}), the internal pull down on the SS pin is released, and the 1.5-mA adaptive soft-start current source is activated. This 1.5-mA pull-up almost immediately pulls the SS pin to 0.75 V (V_{VSENSE}) to bypass the initial 25% of dead time during a traditional 0 V to Vregulation SS ramp. Once the SS pin has reached the voltage on VSENSE, the 10-µA soft-start current (I_{SS}) takes over. Thus, through the selection of the soft-start capacitor (C_{SS}), the effective soft-start time (t_{SS}) may be easily programmed based on the equation below.

$$t_{SS} = C_{SS} \times \left(\frac{2.25V}{10\mu A} \right) \tag{20}$$

Often, a system restart is desired following a brief shut-down. In such a case, VSENSE may still have substantial voltage if V_{OUT} has not fully discharged or if high line has peak charged C_{OUT}. To eliminate the delay caused by charging C_{SS} from 0 V up to the pre-charged V_{VSENSE} with only the 10-µA current source and minimize any further output voltage sag, the adaptive soft start uses a 1.5-mA current source to rapidly charge C_{SS} to V_{VSENSE}, after which time the 10-µA source controls the V_{SS} accent to the desired soft-start ramp rate. In such a case, t_{SS} is estimated as follows:

$$t_{SS} = C_{SS} \times \left(\frac{3V - V_{VSENSE0}}{10\mu A} \right) \tag{21}$$

where $V_{VSENSE0}$ is the voltage at VSENSE at the moment a soft start or restart is initiated.

NOTE

For soft start to be effective and avoid overshoot on V_{OUT}, the SS ramp must be slower than the voltage-loop control response. Choose $C_{SS} \geq C_{VZ}$ to ensure this.

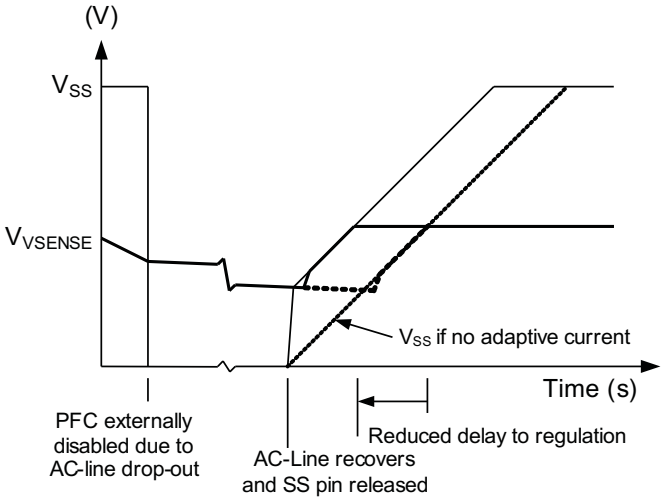

Figure 21. Soft-Start Ramp Rate

PFC Start-Up Hold Off

An additional feature designed into the UCC28070A is the “Start-Up Hold Off” logic that prevents the device from initiating a soft-start cycle until the VAO is below the zero-power threshold (0.75 V). This feature ensures that the SS cycle will initiate from zero-power and zero duty-cycle while preventing the potential for any significant inrush currents due to stored charge in the VAO compensation network.

Output Over-Voltage Protection (OVP)

Because of the high voltage output and a limited design margin on the output capacitor, output over-voltage protection is essential for PFC circuits. The UCC28070A implements OVP through the continuous monitoring of the VSENSE voltage. In the event V_{VSENSE} rises above 106% of regulation (3.18 V), the GDx outputs are immediately disabled to prevent the output voltage from reaching excessive levels. Meanwhile the CAOx outputs are pulled low in order to ensure a controlled recovery starting from 0% duty-cycle after an OVP fault is released. Once the V_{VSENSE} voltage has dropped below 3.08 V, the PWM operation resumes normal operation.

Zero-Power Detection

In order to prevent undesired performance under no-load and near no-load conditions, the UCC28070A zero-power detection comparator is designed to disable both GDA and GDB output in the event the VAO voltage falls below 0.75 V. The 150 mV of hysteresis ensures that the output remains disabled until the VAO has nearly risen back into the linear range of the multiplier (VAO ≥ 0.9 V).

Thermal Shutdown

In order to protect the power supplies from silicon failures at excessive temperatures, the UCC28070A has an internal temperature-sensing comparator that shuts down nearly all of the internal circuitry, and disables the GDA and GDB outputs, if the die temperature rises above 160°C. Once the die temperature falls below 140°C, the device brings the outputs up through a typical soft start.

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Current Loop Compensation

The UCC28070A incorporates two identical and independent transconductance-type current-error amplifiers (one for each phase) with which to control the shaping of the PFC input current waveform. The current-error amplifier (CA) forms the heart of the embedded current control loop of the boost PFC pre-regulator, and is compensated for loop stability using familiar principles [4, 5]. The output of the CA for phase-A is CAOA, and that for phase-B is CAOB. Since the design considerations are the same for both, they are collectively referred to as CAOx, where the "x" may be "A" or "B".

In a boost PFC pre-regulator, the current control loop comprises the boost power plant stage, the current sensing circuitry, the wave-shape reference, the PWM stage, and the CA with compensation components. The CA compares the average boost inductor current sensed with the wave-shape reference from the multiplier stage and generates an output current proportional to the difference.

This CA output current flows through the impedance of the compensation network generating an output voltage, V_{CAO}, which is then compared with a periodic voltage ramp to generate the PWM signal necessary to achieve PFC.

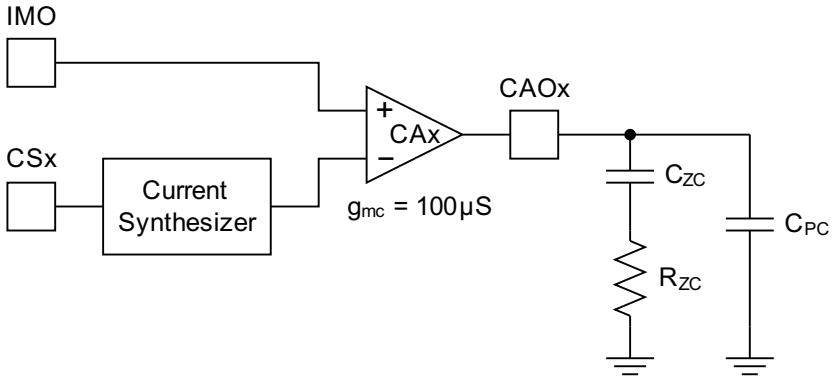

Figure 22. Current Error Amplifier With Type II Compensation

For frequencies above boost LC resonance and below f_{PWM}, the small-signal model of the boost stage, which includes current sensing, can be simplified to:

$$\frac{v_{RS}}{v_{CA}} = \frac{Vout \times R_S / N_{CT}}{\Delta V_{RMP} \times k_{SYNC} \times s \times L_B} \tag{22}$$

where L_B = mid-value boost inductance, R_S = CT sense resistor, N_{CT} = CT turns ratio, V_{OUT} = average output voltage, $\Delta V_{RMP} = 4V_{pk\text{-}pk}$ amplitude of the PWM voltage ramp, k_{SYNC} = ramp reduction factor (if PWM frequency is synchronized to an external oscillator; $k_{SYNC} = 1$ otherwise), s = Laplace complex variable

An $R_{ZC}C_{ZC}$ network is introduced on CAOx to obtain high gain for the low-frequency content of the inductor current signal, but reduced flat gain above the zero frequency out to f_{PWM} to attenuate the high-frequency switching ripple content of the signal (thus averaging it).

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The switching ripple voltage should be attenuated to less than 1/10 of the ΔV_{RMP} amplitude so as to be considered “negligible” ripple.

Thus, CAOx gain at f_{PWM} is:

$$g_{mc} Rzc \le \frac{\Delta V_{RMP} \times k_{SYNC} / 10}{\Delta I_{LB} \times R_S / N_{CT}} \tag{23}$$

where ΔI_{LB} is the maximum peak-to-peak ripple current in the boost inductor, and g_{mc} is the transconductance of the CA, 100 µS.

$$Rzc \le \frac{4V \times N_{CT}}{10 \times 100\mu S \times \Delta I_{LB} \times R_S} \tag{24}$$

The current-loop cross-over frequency is then found by equating the open loop gain to 1 and solving for f_{CXO}:

$$f_{CXO} = \frac{Vout \times R_S / N_{CT}}{\Delta V_{RMP} \times k_{SYNC} \times 2\pi \times L_B} \times g_{mc} Rzc \tag{25}$$

C_{CZ} is then determined by setting $f_{ZC} = f_{CXO} = 1/(2\pi x R_{ZC} x C_{ZC})$ and solving for C_{ZC}. At $f_{ZC} = f_{CXO}$, a phase margin of 45° is obtained at f_{CXO}. Greater phase margin may be had by placing $f_{ZC} < f_{CXO}$.

An additional high-frequency pole is generally added at f_{PWM} to further attenuate ripple and noise at f_{PWM} and higher. This is done by adding a small-value capacitor, C_{pc}, across the $R_{zc}C_{zc}$ network.

$$Cpc = \frac{1}{2\pi \times f_{PWM} \times Rzc} \tag{26}$$

The procedure above is valid for fixed-value inductors.

NOTE

If a “swinging-choke” boost inductor (inductance decreases with increasing current) is used, f_{CXO} varies with inductance, so C_{ZC} should be determined at maximum inductance.

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Voltage Loop Compensation

The outer voltage control loop of the dual-phase PFC controller functions the same as with a single-phase controller, and compensation techniques for loop stability are standard [4]. The bandwidth of the voltage-loop must be considerably lower than the twice-line ripple frequency (f_{2LF}) on the output capacitor, to avoid distortion-causing correction to the output voltage. The output of the voltage-error amplifier (VA) is an input to the multiplier, to adjust the input current amplitude relative to the required output power. Variations on VAO within the bandwidth of the current loops will influence the wave-shape of the input current. Since the low-frequency ripple on C_{OUT} is a function of input power only, its peak-to-peak amplitude is the same at high-line as at low-line. Any response of the voltage-loop to this ripple will have a greater distorting effect on high-line current than on low-line current. Therefore, the allowable percentage of 3rd-harmonic distortion on the input current contributed by VAO should be determined using high-line conditions.

Because the voltage-error amplifier (VA) is a transconductance type of amplifier, the impedance on its input has no bearing on the amplifier gain, which is determined solely by the product of its transconductance (g_{mv}) with its output impedance (Z_{OV}). Thus the VSENSE input divider-network values are determined separately, based on criteria discussed in the VINAC section. Its output is the VAO pin.

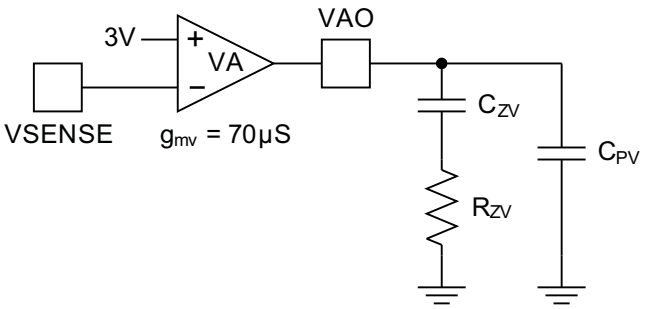

Figure 23. Voltage Error Amplifier With Type II Compensation

The twice-line ripple voltage component of VSENSE must be sufficiently attenuated and phase-shifted at VAO to achieve the desired level of 3rd-harmonic distortion of the input current wave-shape [4]. For every 1% of 3rd-harmonic input distortion allowable, the small-signal gain $G_{VEA} = V_{VAOpk} / v_{SENSEpk} = g_{mv} x Z_{OV}$ at the twice-line frequency should allow no more than 2% ripple over the full VAO voltage range. In the UCC28070A, V_{VAO} can range from 1 V at zero load power to ~4.2 V(see note below) at full load power for a ΔV_{VAO} = 3.2 V, so 2% of 3.2 V is 64-mV peak ripple.

NOTE

Although the maximum VAO voltage is clamped at 5 V, at full load V_{VAO} may vary around an approximate center point of 4.2 V to compensate for the effects of the quantized feed-forward voltage in the multiplier stage (see Multiplier Section for details). Therefore, 4.2 V is the proper voltage to use to represent maximum output power when performing voltage-loop gain calculations.

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The output capacitor maximum low-frequency zero-to-peak ripple voltage is closely approximated by:

$$v_{0\,pk} = \frac{Pin_{avg} \times X_{Cout}}{Vout_{avg}} = \frac{Pin_{avg}}{Vout_{avg} \times 2\pi \times f_{2LF} \times Cout} \tag{27}$$

where $P_{IN(avg)}$ is the total maximum input power of the interleaved-PFC pre-regulator, $V_{OUT(avg)}$ is the average output voltage and C_{OUT} is the output capacitance.

$V_{SENSEpk} = v_{opk} x k_R$, where k_R is the gain of the resistor-divider network on VSENSE.

Thus, for k_{3rd}% of allowable 3rd-harmonic distortion on the input current attributable to the VAO ripple,

$$Z_{OV(f_{2LF})} = \frac{k_{3rd} \times 64mV \times Vout_{avg} \times 2\pi f_{2LF} \times Cout}{g_{mv} \times k_R \times Pin_{avg}} \tag{28}$$

This impedance on VAO is set by a capacitor (Cpv), where $C_{PV} = 1/(2\pi f_{2LF} x Z_{OV}(f_{2LF}))$ therefore,

$$Cpv = \frac{g_{mv} \times k_R \times Pin_{avg}}{k_{3rd} \times 64mV \times Vout_{avg} \times (2\pi f_{2LF})^2 \times Cout} \tag{29}$$

The voltage-loop unity-gain cross-over frequency (f_{VXO}) may now be solved by setting the open-loop gain equal to 1:

$$Tv(f_{VXO}) = G_{BST} \times G_{VEA} \times k_R = \left(\frac{Pin_{avg} \times X_{Cout}}{\Delta V_{VAO} \times Vout_{avg}} \right) \times \left(g_{mv} \times X_{Cpv} \right) \times k_R = 1 \tag{30}$$

so,

$$f_{VXO}{}^2 = \frac{g_{mv} \times k_R \times Pin_{avg}}{\Delta V_{VAO} \times Vout_{avg} \times (2\pi)^2 \times Cpv \times Cout} \tag{31}$$

The "zero-resistor" (R_{ZV}) from the zero-placement network of the compensation may now be calculated. Together with C_{PV}, R_{ZV} sets a pole right at f_{VXO} to obtain 45° phase margin at the cross-over.

Thus,

$$Rzv = \frac{1}{2\pi f_{VXO} \times Cpv} \tag{32}$$

Finally, a zero is placed at or below $f_{VXO}/6$ with capacitor C_{ZV} to provide high gain at dc but with a breakpoint far enough below f_{VXO} so as not to significantly reduce the phase margin. Choosing $f_{VXO}/10$ allows one to approximate the parallel combination value of C_{ZV} and C_{PV} as C_{ZV}, and solve for C_{ZV} simply as:

$$Czv = \frac{10}{2\pi f_{VXO} \times Rzv} \approx 10 \times Cpv \tag{33}$$

By using a spreadsheet or math program, C_{ZV}, R_{ZV}, and C_{PV} may be manipulated to observe their effects on f_{VXO} and phase margin and %-contribution to 3rd-harmonic distortion (see note below). Also, phase margin may be checked as $P_{IN(avg)}$ level and system parameter tolerances vary.

NOTE

The percent of 3rd-harmonic distortion calculated in this section represents the contribution from the f_{2LF} voltage ripple on C_{OUT} only. Other sources of distortion, such as the current-sense transformer, the current synthesizer stage, even distorted V_{IN}, etc., can contribute additional 3rd and higher harmonic distortion.

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Advanced Design Techniques

Current Loop Feedback Configuration (Sizing of the Current Transformer Turns Ratio and Sense Resistor (R_S)

A current-sense transformer (CT) is typically used in high-power applications to sense inductor current while avoiding significant losses in the sensing resistor. For average current-mode control, the entire inductor current waveform is required; however low-frequency CTs are obviously impracticable. Normally, two high-frequency CTs are used, one in the switching leg to obtain the up-slope current and one in the diode leg to obtain the down-slope current. These two current signals are summed together to form the entire inductor current, but this is not the case for the UCC28070A.

A major advantage of the UCC28070A design is the current synthesis function, which internally recreates the inductor current down-slope during the switching period off-time. This eliminates the need for the diode-leg CT in each phase, significantly reducing space, cost and complexity. A single resistor programs the synthesizer down slope, as previously discussed in the Current Synthesizer section.

A number of trade-offs must be made in the selection of the CT. Various internal and external factors influence the size, cost, performance, and distortion contribution of the CT.

These factors include, but are not limited to:

- Turns-ratio (N_{CT})
- Magnetizing inductance (L_M)
- Leakage inductance (L_{LK})
- Volt-microsecond product (Vμs)
- Distributed capacitance (C_d)
- Series resistance (R_{SER})
- External diode drop (V_D)
- External current sense resistor (R_S)
- External reset network

Traditionally, the turns-ratio and the current sense resistor are selected first. Some iterations may be needed to refine the selection once the other considerations are included.

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In general, 50 ≤ N_{CT} ≤ 200 is a reasonable range from which to choose. If N_{CT} is too low, there may be high power loss in R_S and insufficient L_M. If too high, there could be excessive L_{LK} and C_d. (A one-turn primary winding is assumed.)

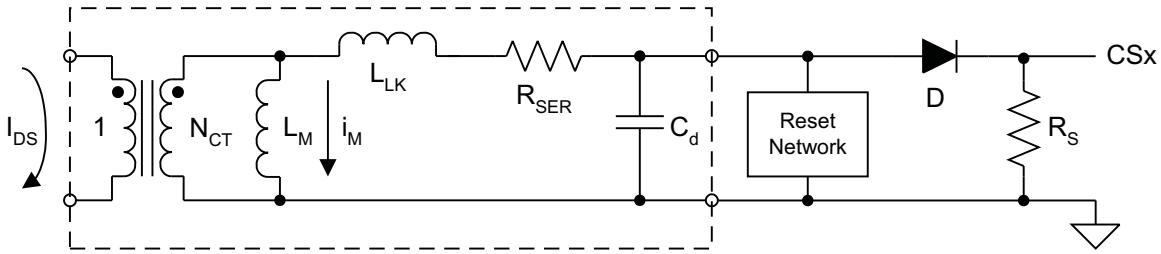

Figure 24. Current Sense Transformer Equivalent Circuit

A major contributor to distortion of the input current is the effect of magnetizing current on the CT output signal (i_{RS}). A higher turns-ratio results in a higher L_M for a given core size. L_M should be high enough that the magnetizing current (i_M) generated is a very small percentage of the total transformed current. This is an impossible criterion to maintain over the entire current range, because i_M unavoidably becomes a larger fraction of i_{RS} as the input current decreases toward zero. The effect of i_M is to "steal" some of the signal current away from R_S, reducing the CSx voltage and effectively understating the actual current being sensed. At low currents, this understatement can be significant and CAOx increases the current-loop duty-cycle in an attempt to correct the CSx input(s) to match the IMO reference voltage. This unwanted correction results in overstated current on the input wave shape in the regions where the CT understatement is significant, such as near the ac line zero crossings. It can affect the entire waveform to some degree under the high line, light-load conditions.

The sense resistor R_S is chosen, in conjunction with N_{CT}, to establish the sense voltage at CSx to be about 3 V at the center of the reflected inductor ripple current under maximum load. The goal is to maximize the average signal within the common-mode input range V_{CMCAO} of the CAOx current-error amplifiers, while leaving room for the peaks of the ripple current within V_{CMCAO}. The design condition should be at the lowest maximum input power limit as determined in the Multiplier Section. If the inductor ripple current is so high as to cause V_{CSx} to exceed V_{CMCAO}, then R_S or N_{CT} or both must be adjusted to reduce peak V_{CSx}, which could reduce the average sense voltage center below 3 V. There is nothing wrong with this situation; but be aware that the signal is more compressed between full- and no-load, with potentially more distortion at light loads.

The matter of volt-second balancing is important, especially with the widely varying duty-cycles in the PFC stage. Ideally, the CT is reset once each switching period; that is, the off-time Vμs product equals the on-time Vμs product. (Because a switching period is usually measured in microseconds, it is convenient to convert the volt-second product to volt-microseconds to avoid sub-decimal numbers.) On-time Vμs is the time-integral of the voltage across L_M generated by the series elements R_{SER}, L_{LK}, D, and R_S. Off-time Vμs is the time-integral of the voltage across the reset network during the off-time. With passive reset, Vμs-off is unlikely to exceed Vμs-on. Sustained unbalance in the on or off Vμs products will lead to core saturation and a total loss of the current-sense signal. Loss of V_{CSx} causes V_{CAOx} to quickly rise to its maximum, programming a maximum duty-cycle at any line condition. This, in turn causes the boost inductor current to increase without control, until the system fuse or some component failure interrupts the input current.

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It is vital that the CT has plenty of Vμs design-margin to accommodate various special situations where there to be several consecutive maximum duty-cycle periods at maximum input current, such as during peak current limiting.

Maximum Vμs(on) can be estimated by:

$$V_{\mu(on)max} = t_{ON(max)} \times \left(V_{RS} + V_D + V_{RSER} + V_{LK}\right) \quad (34)$$

where all factors are maximized to account for worst-case transient conditions and $t_{ON(max)}$ occurs during the lowest dither frequency when frequency dithering is enabled. For design margin, a CT rating of ~5*Vμs(on)max or higher is suggested. The contribution of V_{RS} varies directly with the line current. However, V_D may have a significant voltage even at near-zero current, so substantial Vμs(on) may accrue at the zero-crossings where the duty-cycle is maximum. V_{RSER} is the least contributor, and often can be neglected if $R_{SER} << R_S$. V_{LK} is developed by the di/dt of the sensed current, and is not observable externally. However, its impact is considerable, given the sub-microsecond rise-time of the current signal plus the slope of the inductor current. Fortunately, most of the built-up Vμs across L_M during the on-time is removed during the fall-time at the end of the duty-cycle, leaving a lower net Vμs(on) to be reset during the off-time. Nevertheless, the CT must, at the very minimum, be capable of sustaining the full internal Vμs(on)max built up until the moment of turn-off within a switching period.

Vμs(off) may be generated with a resistor or zener diode, using the i_M as bias current.

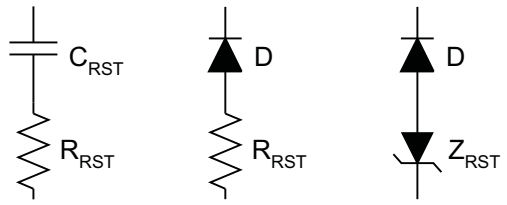

Figure 25. Possible Reset Networks

In order to accommodate various CT circuit designs and prevent the potentially destructive result due to CT saturation, the UCC28070A's maximum duty-cycle needs to be programmed such that the resulting minimum off-time accomplishes the required worst-case reset. (See the PWM Frequency and Duty-Cycle Clamp section of the data sheet for more information on sizing R_{DMX}) Be aware that excessive C_d in the CT can interfere with effective resetting, because the maximum reset voltage is not reached until after 1/4-period of the CT self-resonant frequency. A higher turns-ratio results in higher C_d [3], so a trade-off between N_{CT} and D_{MAX} must be made.

The selected turns-ratio also affects L_M and L_{LK}, which vary proportionally to the square of the turns. Higher L_M is good, while higher L_{LK} is not. If the voltage across L_M during the on-time is assumed to be constant (which it is not, but close enough to simplify) then the magnetizing current is an increasing ramp.

This upward ramping current subtracts from i_{RS}, which affects V_{CSx} especially heavily at the zero-crossings and light loads, as stated earlier. With a reduced peak at V_{CSx}, the current synthesizer starts the down-slope at a lower voltage, further reducing the average signal to CAOx and further increasing the distortion under these conditions. If low input current distortion at very light loads is required, special mitigation methods may need to be developed to accomplish that goal.

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Current Sense Offset and PWM Ramp for Improved Noise Immunity

To improve noise immunity at extremely light loads, a PWM ramp with a dc offset is recommended to be added to the current sense signals. Electrical components R_{TA}, R_{TB}, R_{OA}, R_{OB}, C_{TA}, C_{TB}, D_{PA1}, D_{PA2}, D_{PB1}, D_{PB1} C_{TA}, C_{TB} form a PWM ramp that is activated and deactivated by the gate drive outputs of the UCC28070A. Resistor R_{OA} and R_{OB} add a dc offset to the CS resistors (R_{SA} and R_{SB}).

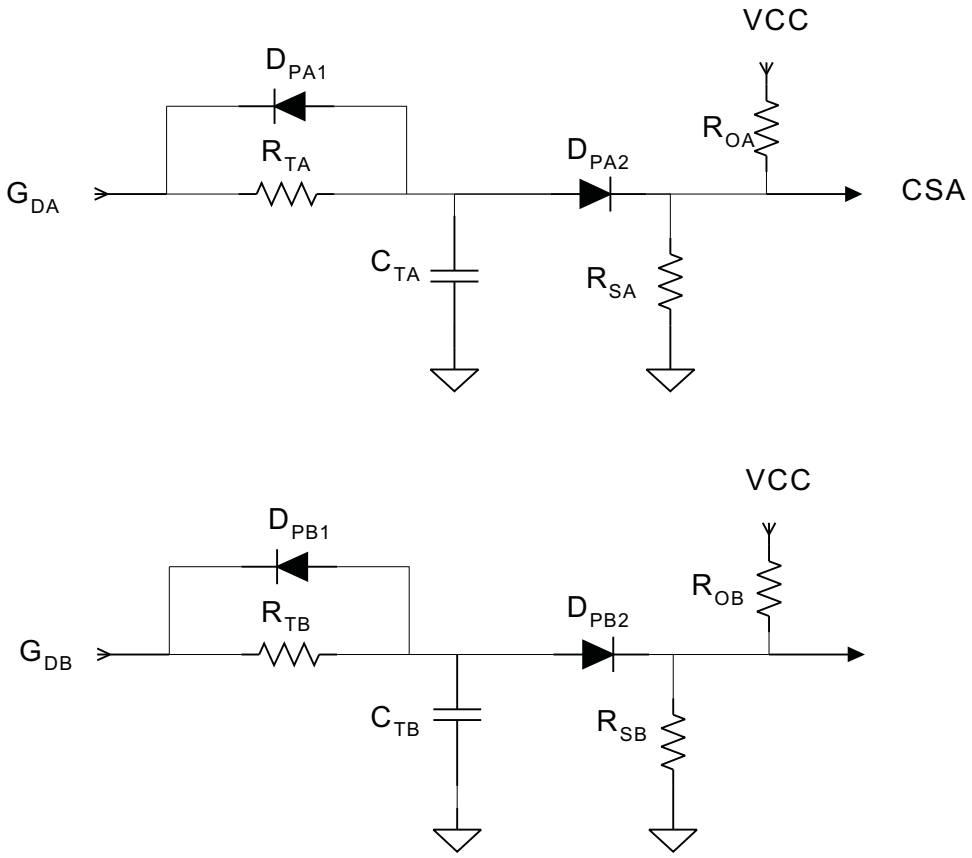

Figure 26. PWM Ramp and Offset Circuit

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When the inductor current becomes discontinuous the boost inductors ring with the parasitic capacitances in the boost stages. This inductor current rings through the CTs causing a false current sense signal. Please refer to the following graphical representation of what the current sense signal looks like when the inductor current goes discontinuous.

NOTE

The inductor current and RS may vary from this graphical representation depending on how much inductor ringing is in the design when the unit goes discontinuous.

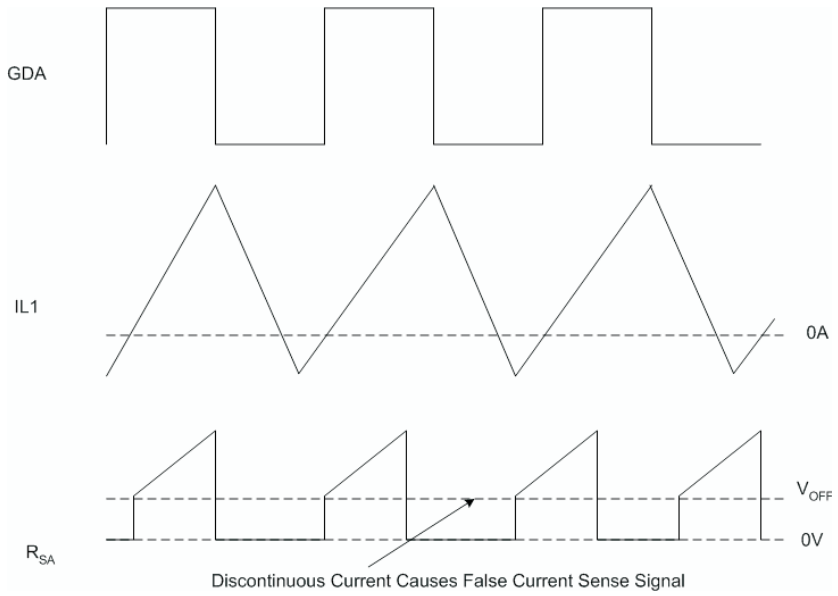

Figure 27. False Current Sense Signal

To counter for the offset (V_{OFF}) just requires adjusting resistors R_{OA} and R_{OB} to ensure that when the unit goes discontinuous the current sense resistor is not seeing a positive current when it should be zero. Setting the offset to 120 mV is a good starting point and may need to be adjusted based on individual design criteria.

$$R_{SA} = R_{SB} \tag{35}$$

$$R_{OA} = R_{OB} = \frac{\left(V_{VCC} - V_{OFF}\right)R_{SA}}{V_{OFF}} \tag{36}$$

A small PWM ramp that is equal to 10% of the maximum current sense signal (V_S) less the offset can then be added by properly selecting R_{TA}, R_{TB}, C_{TA} and C_{TB}.

$$R_{TA} = R_{TB} = \frac{\left(V_{VCC} - (V_S \times 0.1 - V_{OFF}) + V_{DA2}\right)R_{SA}}{V_S \times 0.1 - V_{OFF}} \tag{37}$$

$$C_{TA} = C_{TB} = \frac{1}{R_{TA} \times f_S \times 3} \tag{38}$$

Recommended PCB Device Layout

Interleaved PFC techniques dramatically reduce input and output ripple current caused by the PFC boost inductor, which allows the circuit to use smaller and less expensive filters. To maximize the benefits of interleaving, the output filter capacitor should be located after the two phases allowing the current of each phase to be combined together before entering the boost capacitor. Similar to other power management devices, when laying out the PCB it is important to use star grounding techniques and to keep filter and high frequency bypass capacitors as close to device pins and ground as possible. To minimize the possibility of interference caused by magnetic coupling from the boost inductor, the device should be located at least 1 inch away from the boost inductor. It is also recommended that the device not be placed underneath magnetic elements.

References

1. O'Loughlin, Michael, *"An Interleaving PFC Pre-Regulator for High-Power Converters"*, Texas Instruments, Inc. 2006 Unitrode Power Supply Seminar, Topic 5
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3. Creel, Kirby *"Measuring Transformer Distributed Capacitance"*, White Paper, Datatronic Distribution, Inc. website: http://www.datatronics.com/pdf/distributed_capacitance_paper.pdf
4. L. H. Dixon, *"Optimizing the Design of a High Power Factor Switching Preregulator"*, Unitrode Power Supply Design Seminar Manual SEM700, 1990. Texas Instruments Literature Number SLUP093
5. L. H. Dixon, *"High Power Factor Preregulator for Off-Line Power Supplies"*, Unitrode Power Supply Design Seminar Manual SEM600, 1988. Texas Instruments Literature Number SLUP087

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
UCC28070APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28070APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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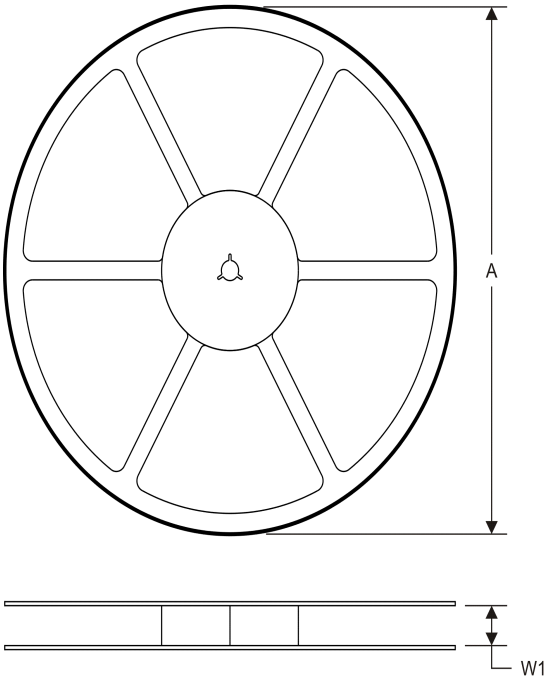
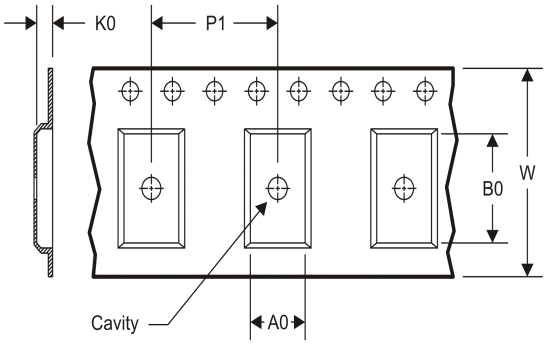
REEL DIMENSIONS



TAPE DIMENSIONS



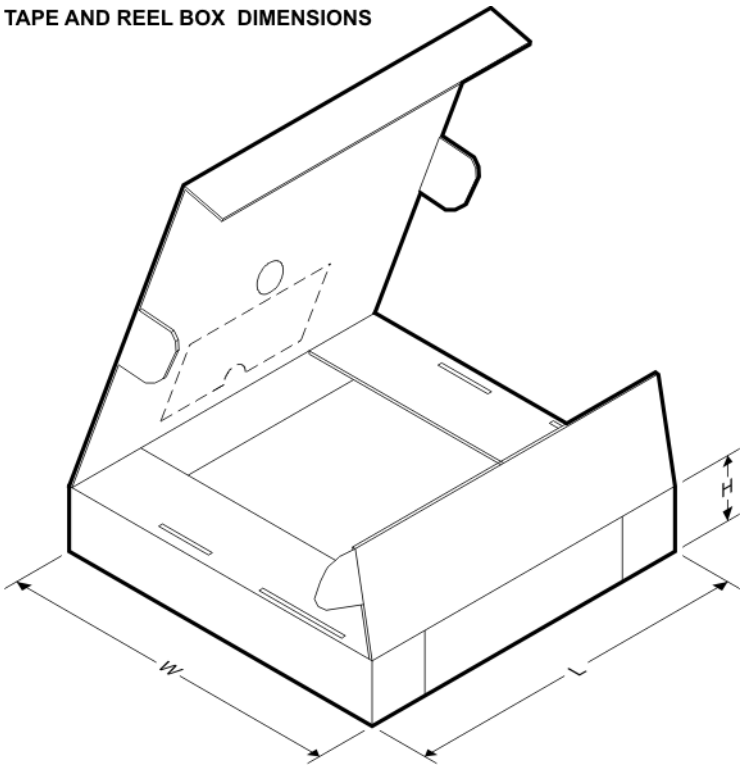
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28070APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

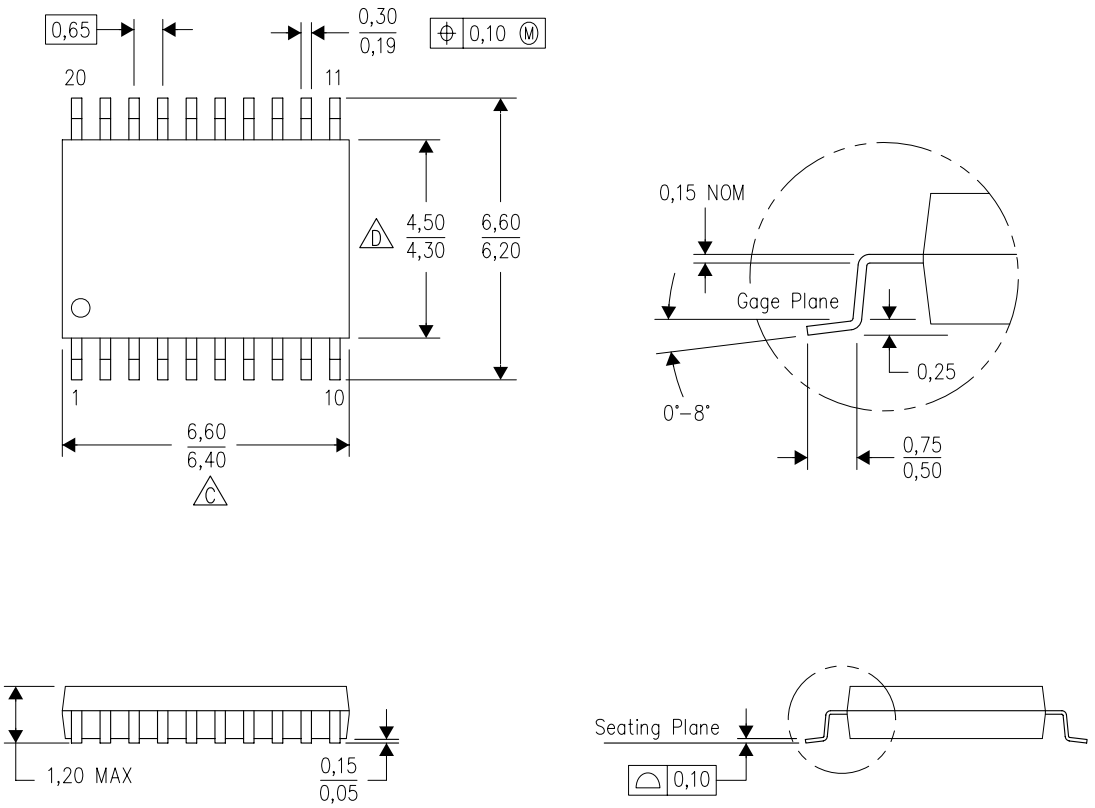
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28070APWR	TSSOP	PW	20	2000	367.0	367.0	38.0

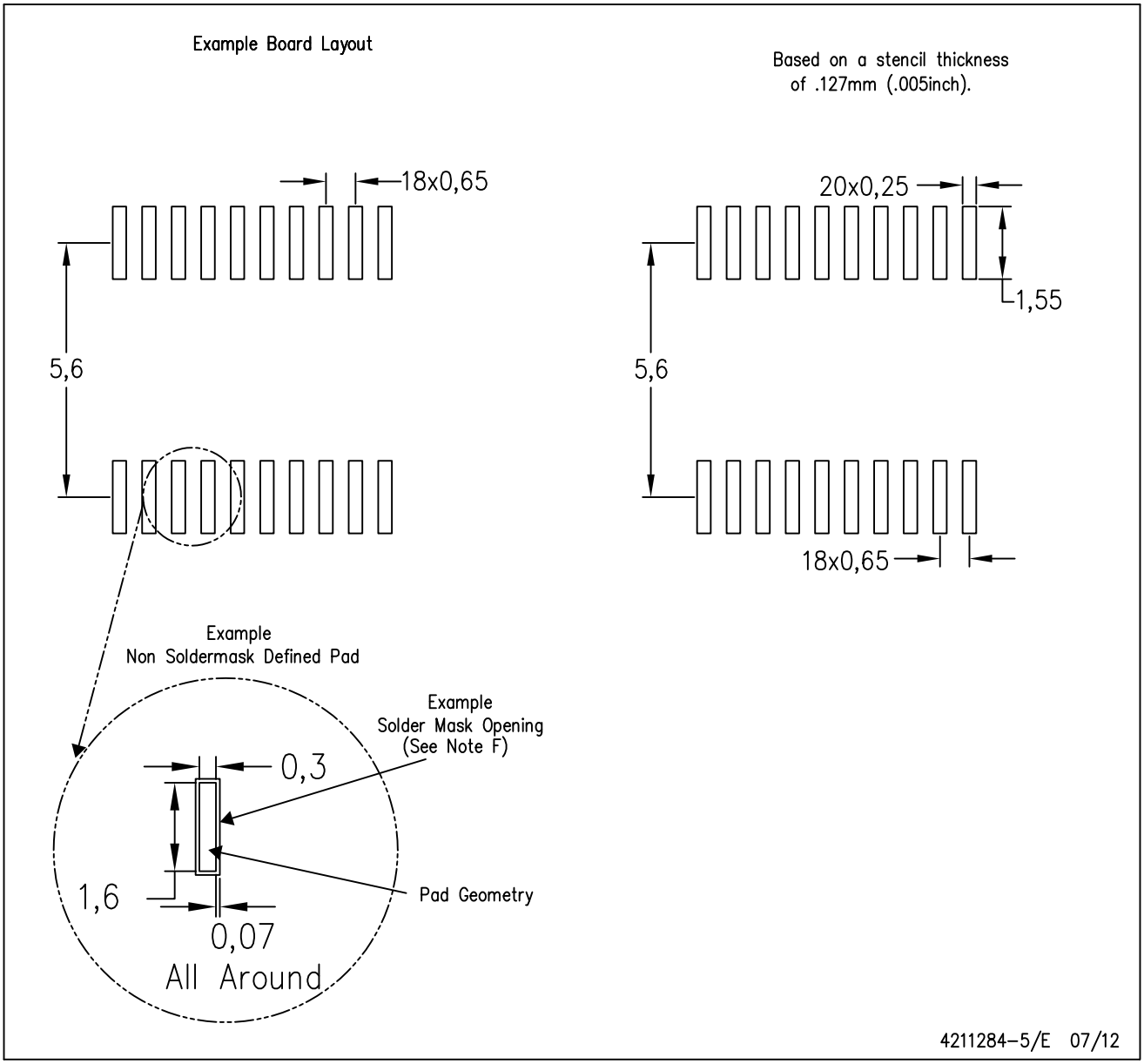
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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